PERIYAR CENTENARY POLYTECHNIC COLLEGE

PERIYAR NAGAR – VALLAM – THANJAVUR – 613 403

(AUTONOMOUS INSTITUTION)

DIPLOMA IN ELECTRONICS
AND
COMMUNICATION ENGINEERING

SYLLABUS

ECD/21/00

SEMESTER SYSTEM

D– SCHEME

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PERIYAR CENTENARY POLYTECHNIC COLLEGE
VALLAM – 613 403, THANJAVUR

Department of Electronics and Communication Engineering

Programme Advisory Committee (PAC)
Syllabus Revision

Chairperson

Dr.R.Malliga
Principal
Periyar Centenary Polytechnic College
Vallam – 613 403, Thanjavur.

Convener

Dr.A.Hemalatha
Vice-Principal & HOD/ECE
Periyar Centenary Polytechnic College
Vallam – 613 403, Thanjavur.

Members

1	Ms.S.Dhanalakshmi Manager/Quality Avalon Technology & Services B7&B8, First Main Road, MEPZ – SEZ, Tambaram, Chennai – 600 045	5	Dr. V. Violet Juli Associate Professor / ECE Periyar Maniammai Institute of Science and Technology, Vallam, Thanjavur
2	Mr. K.Amirtha Ganesh Director Armadha Industrial Automation No. 47,HIG, New Housing Unit Thanjavur	6	Ms.G.Bhuvaneswari Assistant Executive Engineer. TNEB Thanjavur
3	Er. S.M. Sethupathy Embedded Developer Logiczen Career Development Center Near Meenakshi Hospital Thanjavur	7	Ms. G.Roja Lecturer/ECE Periyar Centenary Polytechnic College Vallam- 613 403, Thanjavur
4	Ms. I.Muthumani P.G HOD/ECE Government College of Engineering Thirunelveli	8	Mr. M. Ramesh Lecturer/ECE Periyar Centenary Polytechnic College Vallam- 613 403, Thanjavur

PERIYAR CENTENARY POLYTECHNIC COLLEGE

Periyar Nagar, Vallam – 613 403, Thanjavur

AUTONOMOUS INSTITUTION

VISION

Periyar Centenary Polytechnic College aspires to be recognized as one of the leaders in imparting quality technical education and strives to prepare rural students with excellent technical and life skills for the benefit of the stakeholders and society at large.

MISSION

M1: To impart quality technical education to the students and equip them with knowledge, skills and attitudes that will lead to successful employment in industry/business, entrepreneurship and higher education.

M2: To provide conducive learning environment and adopt well-structured teaching – learning practices to make the students technically competent.

M3: To strengthen the collaboration with industry and community for career development, placement and extension services.

M4: To develop the personality of the students and identify themselves as good individuals, professionals and responsible citizens with ethical values.

M5: To inculcate lifelong learning skills to face challenges with innovations.

PROGRAM OUTCOMES (POs)

1. **Basic and Discipline specific knowledge:** Apply knowledge of basic mathematics, science and engineering fundamentals and engineering specialization to solve the engineering problems.
2. **Problem analysis:** Identify and analyse well-defined engineering problems using codified standard methods.
3. **Design/ development of solutions:** Design solutions for well-defined technical problems and assist with the design of systems components or processes to meet specified needs.
4. **Engineering Tools, Experimentation and Testing:** Apply modern engineering tools and appropriate technique to conduct standard tests and measurements.
5. **Engineering practices for society, sustainability and environment:** Apply appropriate technology in context of society, sustainability, environment and ethical practices.
6. **Project Management:** Use engineering management principles individually, as a team member or a leader to manage projects and effectively communicate about well-defined engineering activities.
7. **Life-long learning:** Ability to analyze individual needs and engage in updating in the context of technological changes.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

Create excellent diploma engineers capable of facing the contemporary and future challenges in the field of Electronics and Communication Engineering through students centred teaching learning practices with social responsibility.

MISSION

M1: To impart quality education and training with competitive curriculum and prepare the students to excel in professional career.

M2: To provide a creative environment and equip the students with technical skills and knowledge through well-structured teaching - learning process and to achieve academic excellence.

M3: To strengthen the soft skills, especially of rural students through co-curricular and extracurricular activities.

M4: To create awareness and thirst for lifelong learning through interactions with outside world regarding contemporary issues, technological trends and entrepreneurship.

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

PEO1: Our Diploma graduates will have the ability to work in industry, institute and as an entrepreneur in Electronics and Communication Engineering field , pursue higher education and develop independent and lifelong learning skills for continuous professional development.

PEO2: Our Diploma graduates will be able to demonstrate technical competence in their chosen field of employment by identifying, analysing and providing engineering solutions using current techniques and tools.

PEO3: Our Diploma graduates will be able to communicate effectively and practice professional ethics and social responsibility in their career.

PROGRAMME SPECIFIC OUTCOMES (PSOs)

PSO1: Understand the fundamental concepts and techniques of Electronics and communication Engineering to design and develop the Electronics, Digital, Microcontroller and communication systems.

PSO2: Apply the technical knowledge and skills in VLSI design, embedded systems and advanced communication systems using appropriate tools.

PSO3: Analyze and develop relevant solutions using domain knowledge with respect to design and analysis using hardware and software tools.

OUTCOME BASED EDUCATION(OBE)

Our institution is practicing Outcome Based Education (OBE) which is a student centered instruction model that focuses on measuring student performance through outcomes. Outcomes include knowledge, skills and attitudes.

In the OBE model, the required knowledge and skill sets for a particular diploma programme is predetermined and the students are evaluated for all the required parameters (Outcomes) during the course of the program.

The OBE model measures the progress of the graduate in four parameters, which are

- Program Educational Objectives (PEO)
- Program Specific Outcomes (PSO)
- Program Outcomes (PO)
- Course Outcomes (CO)

Program Educational Objectives (PEOs) are broad statements that describe the career and professional accomplishments that the program is preparing the graduates to achieve. PEO's are measured 4-5 years after graduation.

Program Specific Outcomes (PSOs) are the statements that describe what the graduates of specific engineering program should be able to do.

Program Outcomes (POs) are narrower statements that describe what students are expected to know and be able to do by the time of graduation.

Course Outcomes(COs) are the measurable parameters which evaluates each students performance for each course that the student undertakes in every semester. The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. According to revised Bloom's taxonomy, the levels in cognitive domain are as follows:

Level	Descriptor	Level of attainment
1	Remembering	Recalling from memory of previously learned material
2	Understanding	Explaining ideas or concepts
3	Applying	Using information in another familiar situation
4	Analyzing	Breaking information into part to explore Understandings and relationships
5	Evaluating	Justifying a decision or course of action
6	Creating	Generating new ideas, products or new ways of Viewing things.

DIPLOMA PROGRAMME IN ENGINEERING / TECHNOLOGY
(Implemented from 2020 -2021)

D SCHEME

RULES AND REGULATIONS

1. Description of the Programme:

a. Full Time (3 years)

The Programme for the Full Time Diploma in Engineering shall extend over a period of three academic years, consisting of 6 semesters***** and the First Year is common to all Engineering Branches.

b. Sandwich (3 1/2 years)

The Programme for the Sandwich Diploma in Engineering shall extend over a period of three and half academic years, consisting of 7 semesters***** and the First Year is common to all Engineering Branches. The courses of three years full time diploma programme being regrouped for academic convenience.

During 4th and/or during 7th semester the students undergo industrial training for six months / one year. Industrial training examination will be conducted after completion of every 6 months of industrial training.

***Each Semester will have 16 weeks duration of studies with 35 hrs / Week for all Diploma Programmes.**

The Curriculum for all the 6 Semesters of Diploma Programme (Engineering & Special Diploma Programmes viz. Modern Office Practice) have been revised and revised curriculum is applicable for the candidates admitted from 2020 - 2021 academic year onwards.

2. Condition for Admission:

Condition for admission to the Diploma Programmes shall be required to have passed in the S.S.L.C Examination of the Board of Secondary Education, Tamil Nadu.

(Or)

The Anglo Indian High School Examination with eligibility for Higher Secondary Course in Tamil Nadu.

(Or)

The Matriculation Examination of Tamil Nadu.

(Or)

Any other Examinations recognized as equivalent to the above by the Board of Secondary Education, Tamil Nadu.

Note: In addition, at the time of admission the candidate will have to satisfy certain minimum requirements, which may be prescribed from time to time

3. Admission to Second year (Lateral Entry):

A pass in HSC (academic) or (vocational) courses mentioned in the Higher Secondary Schools in Tamil Nadu affiliated to the Tamil Nadu Higher Secondary Board with eligibility for University Courses of study or equivalent examination &should have studied the following courses.

A pass in 2 Years ITI with appropriate Trade or Equivalent examination.

Sl.No	Programmes	H.Sc Academic	H.Sc Vocational		Industrial Training Institutes Courses
		Subjects Studied	Subjects Studied		
			Related Subjects	Vocational Subjects	
1	All the Regular and Sandwich Diploma Programmes	Physics and Chemistry as compulsory along with Mathematics / Biology	Maths / Physics / Chemistry	Related Vocational Subjects Theory & Practical	2 years courses to be passed with appropriate Trade
2	Diploma Programme in Modern Office Practice	English & Accountancy English & Elements of Economics English & Elements of Commerce	English & Accountancy English & Elements of Economics English & Management principles & Techniques English & Typewriting	Accountancy & Auditing Banking Business Management, Co – operative Management, International Trade, Marketing& Salesmanship, Insurance & Material Management, Office Secretaryship	-

- For the Diploma Programmes related with Engineering/ Technology, the related / equivalent subjects prescribed along with Practicals may also be taken for arriving the eligibility.
- Programme will be allotted according to merit through counseling by the Principal as per communal reservation.
- For admission to the Modern Office Practice Diploma Programme the candidates studied the related courses will be given first preference.
- Candidates who have studied Commerce courses are not eligible for Engineering Diploma Programmes.

4. Age Limit: No Age limit.

5. Medium of Instruction: English

6. Eligibility for the Award of Diploma:

No candidate shall be eligible for the Diploma unless he/she has undergone the prescribed Programme of study for a period of not less than 3 academic years in any institution affiliated to the State Board of Technical Education and Training, Tamil Nadu, when joined in First Year and two years if joined under Lateral Entry scheme in the second year and passed the prescribed examination.

The minimum and maximum period for completion of Diploma Programmes are as given below:

Diploma Programme	Minimum Period	Maximum Period
Full Time	3 Years	6 Years
Full Time (Lateral Entry)	2 Years	5 Years
Sandwich	3 ½ Years	6 ½ Years

This will come into effect from D Scheme onwards i.e. from the academic year 2020-2021

7. Courses of Study and Curriculum outline:

The courses of study shall be in accordance with the syllabus prescribed from time to time, both in theory and practical courses.

The curriculum outline is given in Annexure - I.

8. Examinations:

Autonomous Examinations in all courses of all the semesters under the scheme of examinations will be conducted at the end of each semester.

The internal assessment marks for all the courses will be awarded on the basis of continuous internal assessment earned during the semester concerned. For each course 25 marks are allotted for internal assessment. Autonomous Examinations are conducted for 100 marks and reduced to 75.

The total marks for result are 75 + 25 = 100 Marks.

9. Continuous Internal Assessment:

A . For Theory Courses

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	-	**25 Marks**
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i) Course Attendance **5 Marks**

(Award of marks for course attendance to each course Theory/Practical will be as per the range given below)

80%	-	83%	1 Mark
84%	-	87%	2 Marks
88%	-	91%	3 Marks
92%	-	95%	4 Marks
96%	-	100%	5 Marks

ii)Test# 10 Marks

3 tests each of 2 hours duration for a total of 50 marks are to be Conducted. Average of these 3 test marks will be taken and the marks to be reduced to: **05 Marks**

The Test – IV is to be the Model Examination covering all the five units and the marks so obtained will be reduced to: **05 Marks**

Test	Units	When to conduct	Marks	Duration
Test – I	Unit I & II	End of 6th week	50	2 hrs
Test – II	Unit III & IV	End of 12th week	50	2 hrs
Test – III	Unit V	End of 15th week	50	2 hrs
Test– IV	**Model Examination - Compulsory** Covering all the 5 units (Autonomous Examination – question paper pattern)	End of 16th Week	100	3 hrs

 # From the Academic Year 2020 – 2021 onwards.

Question Paper Pattern for the Test – I, Test – II and Test - III is as follows. The tests should be conducted by proper schedule. Retest marks should not be considered for internal assessment.

For I Year

Question Pattern (Without Choice):

Part A Type Questions: 6 Questions x1 mark	:	06 marks
Part B Type Questions: 8 Questions x 2 marks	:	16 marks
Part C Type Questions: 4 Questions x 7 marks	:	28 marks
Total	**:**	**50 marks**

For II & III Year

Question Pattern (Without Choice):

Part A Type questions : 5 Questions × 2 marks	:	10 marks
Part B Type questions : 4 Questions × 3 marks	:	12 marks
Part C Type questions : 2 Questions × 14 marks	:	28 marks
Total	**:**	**50 marks**

iii) Assignment **05 marks**

For each course, three assignments are to be given each for 20 marks and the average marks scored should be reduced for 5 marks.

Assignment 1: Written notes in relevant topics from the courses in unit I& II.

Assignment 2: Written notes in relevant topics from the courses in unit III , IV &V.

Assignment 3: Objective type online test to understand the principles and thereby gain in-depth knowledge about the course.

iv) Seminar Presentation **05 Marks**

The students have to select the topics either from their courses or general courses which will help to improve their grasping capacity as well as their capacity to express the course in hand. The students will be allowed to prepare the material for the given topic using the library hour and they will be permitted to present seminar(For First and Second Year, the students will be permitted to present the seminar as a group not exceeding six members and each member of the group should participate in the presentation. For the Third Year, the students should present the seminar individually.) The seminar presentation is mandatory for all theory courses and carries 5 marks for each theory course. The respective course faculty may suggest topics to the students and will evaluate the submitted materials and seminar presentation. (2$^1/_2$ marks for the material submitted in writing and 2$^1/_2$ marks for the seminar presentation). For each course minimum of two seminars are to be given and the average marks scored should be reduced to 5 marks.

All Test Papers, Assignment Papers / Notebooks and the seminar presentation written material after getting the signature with date from the students must be kept in safe custody in the department for verification and audit. It should be preserved for one semester after publication of Autonomous Exam results and produced to the flying squad and the inspection team at the time of inspection/verification.

B. For Practical Courses:

I, II and III Year

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:

a) Attendance (Award of marks same as theory courses)	:	**05 Marks**
b) Procedure/ observation and tabulation/ Other Practical related Work	:	**05 Marks**
c) Tests**#**	:	**10 Marks**
d) Student Centered Learning (SCL) work sheet	:	**05 Marks**
TOTAL		**25 Marks**

 # Tests **10 Marks**

3 tests each of 2 hours duration for a total of 50 marks are to be conducted. Average of these 3 test marks will be taken and the marks to be reduced to: **05 Marks**

The Test – IV is to be the Model Examination covering all the experiments and the marks so obtained will be reduced to: **05 Marks**

- All the Experiments/Exercises indicated in the syllabus should be completed and the same to be given for final Autonomous examinations.
- The observation note book / manual should be maintained. The observation note book / manual with sketches, circuits, program, reading and calculation written by the students manually depends upon the practical course during practical classes should be evaluated properly during the practical class hours with date.
- The Record work for every completed exercise should be submitted in the subsequent practical classes.
- At the end of the Semester, the average marks of all the exercises should be calculated for 20 marks (including Observation, Tests and SCL work sheet) and the marks awarded for attendance is to be added to arrive at the internal assessment mark for Practical. (20+5=25 marks)
- Only regular students, appearing first time have to submit the duly signed bonafide record note book/file during the Practical Autonomous Examinations.

All the marks awarded for Assignments, Tests, Seminar presentation and Attendance should be entered periodically in the Personal Theory Log Book of the staff, who is handling the theory course. The marks awarded for Observation, SCL work sheet, Tests and Attendance should be entered periodically in the Personal Practical Log Book of the staff, who is handling the practical course.

10. Communication Skill Practical, Computer Application Practical and Physical Education:

The Communication Skill Practical and Computer Application Practical with more emphasis are being introduced in First Year. Much Stress is given to increase the Communicative skill and ICT skill of students. As per the recommendation of MHRD and under Fit India scheme, the Physical education is introduced to encourage students to remain healthy and fit by including physical activities and sports.

11. Project Work and Internship:

The students of all the Diploma Programmes have to do a Project Work as part of the Curriculum and in partial fulfillment for the award of Diploma by the State Board of Technical Education and Training, Tamil Nadu. In order to encourage students to do worthwhile and innovative projects, every year prizes are awarded for the best three projects i.e. institution wise, region wise and state wise**. The Project work must be reviewed twice in the same semester. The project work is approved during the V semester by the properly constituted committee with guidelines.**

a) Internal Assessment Mark for Project Work & Internship:

Project Review I	:	**10 marks**
Project Review II	:	**10 marks**
Attendance	:	**05 marks** (Award of marks same as theory course pattern)

Total	**:**	**25 marks**

Proper record should be maintained for the two Project Reviews and preserved for one semester after the publication of Autonomous Exams results. It should be produced to the flying squad and the inspection team at the time of inspection/verification.

b) Allocation of Marks for Project Work & Internship in Autonomous Examinations:

Demonstration/Presentation	25 marks
Report	25 marks
Viva Voce	30 marks
Internship Report	20 marks

Total	**100* marks**
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*Examination will be conducted for 100 marks and will be converted to 75 marks.

c) Internship Report:

The internship training for a period of two weeks shall be undergone by every candidate at the end of IV / V semester during vacation. The certificate shall be produced along with the internship report for evaluation. The evaluation of internship training shall be done along with final year "Project Work & Internship" for 20 marks. The internship shall be undertaken in any

industry / Government or Private certified agencies which are in social sector / Govt. Skill Centre / Institutions / Schemes.

A neatly prepared PROJECT REPORT as per the format has to be submitted by individual student during the Project Work & Internship Autonomous examination.

12. Industrial Training and Project Work (Architectural Assistantship(SW)

i. Industrial Training

In IV and VII semesters, students should undergo the industrial training under the registered architects without fail. During this period, they should have 80% of attendance. Candidates not fulfilling the above are not eligible to appear for the practical examinations and the candidates should redo the industrial training in the next academic year.

The internal Assessment is based on the monthly report, Weekly report and drawing works completed in training period.

Work diary (internal Assessment)	**25 marks**
Monthly report	5 Marks
Weekly report	5 Marks
Drawing works	10 Marks
Attendance	5 Marks
Total	**25 Marks**

Architect office and studio practice –I &II (IV & VII Sem)

Report writing	60 marks
Viva- voce	40 marks
Total	**100 marks***

*Examination will be conducted for 100 marks and will be converted to 75 marks.

ii. Project work

a) Internal Assessment Mark for Project Work

Project Review I	**10 marks**
Project Review II	**10 marks**
Attendance	**05 marks** (Award of marks same as theory course pattern)
Total	**25 marks**

b) Project work & Viva voce – Autonomous Examination

Project Report	25 marks
Drawing &Presentation	25 marks
Viva Voce	30 marks
Model	20 marks
Total	**100* marks**

*Examination will be conducted for 100 marks and will be converted to 75 marks.

A neatly prepared PROJECT REPORT as per the format has to be submitted by individual student during the project Work & Viva voce Autonomous Examination.

13. Scheme of Examinations:

The Scheme of examinations for courses is given in Annexure - II.

14. Criteria for Pass:

1. No candidate shall be eligible for the award of Diploma unless he/she has undergone the prescribed programme of study successfully in an institution approved by AICTE and affiliated to the State Board of Technical Education & Training, Tamil Nadu and pass all the courses prescribed in the curriculum.

2. A candidate shall be declared to have passed the examination in a course if he/she secures not less than 40% in theory courses and 50% in practical courses out of the total prescribed maximum marks including both the Internal Assessment and the Autonomous Examinations marks put together, subject to the condition that he/she secures at least a minimum of 40 marks out of 100 marks in the Autonomous Theory Examinations and a minimum of 50 marks out of 100 marks in the Autonomous Practical Examinations.

15. Classification of successful candidates:

Classification of candidates who will pass out the final examinations from April 2023 onwards (Joined first year in 2020 -2021) will be done as specified below.

First Class with Superlative Distinction:

A candidate will be declared to have passed in **First Class with Superlative Distinction** if he/she secures not less than 75% of the marks in all the courses and passes all the semesters in the first appearance itself and passes all courses within the stipulated period of study 2/3/3 ½ /4 years [Full time(lateral entry)/Full Time/Sandwich/Part Time) without any break in study.

First Class with Distinction:

A candidate will be declared to have passed in **First Class with Distinction** if he/she secures not less than 75% of the aggregate marks in all the semesters put together and passes all the semesters except the I and II semester in the first appearance itself and passes all courses within the stipulated period of study 2/3/3 ½ /4 years [Full time(lateral entry)/Full Time/Sandwich/Part Time) without any break in study.

First Class:

A candidate will be declared to have passed in **First Class** if he/she secures not less than 60% of the aggregate marks in all the semesters put together and passes all the courses within the stipulated period of study 2 / 3/ 3½ / 4 years [Full time(lateral entry)/ Full Time/Sandwich/Part Time) without any break in study.

Second Class:

All other successful candidates will be declared to have passed in **Second Class**.

The above classifications are also applicable for the Sandwich / Part-Time students who pass out Final Examination from October 2023 /April 2024 onwards (both joined First Year in2020 - 2021)

16. Duration of a period in the Class Time Table:

The duration of each period of instruction is 1 hour and the total period of instruction hours excluding interval and lunch break in a day should be uniformly maintained as 7 hours corresponding to 7 periods of instruction (Theory & Practical)

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‘D’ SCHEME

ANNEXURE – I

CURRICULUM OUTLINE

THIRD SEMESTER

Sl.No	Course Code	Course	Hours Per Week			
			Theory Hours	Tutorial/ Drawing	Practical Hours	Total Hours
1.	ECD310	Electronic Devices and Circuits	5	-	-	5
2.	ECD320	Electrical Circuits and Instrumentation	6	-	-	6
3.	ECD330	Programming in ‘C’	5	-	-	5
4.	ECD340	Electronic Devices and Circuits Practical	-	-	4	4
5.	ECD350	Electrical Circuits and Instrumentation Practical	-	-	4	4
6.	ECD360	Programming in ‘C’ Practical	-	-	4	4
7.	ECD370	Simulation Practical	-	-	4	4
Extra &Co - Curricular Activities		Physical Education	-	2	-	2
		Library	-	1	-	1
		Total	16	3	16	35

FOURTH SEMESTER

Sl.No	Course Code	Course	Hours Per Week			
			Theory Hours	Tutorial/ Drawing	Practical Hours	Total Hours
1.	ECD410	Industrial Electronics	5	-	-	5
2.	ECD420	Communication Engineering	5	-	-	5
3.	ECD430	Analog and Digital Electronics	4	-	-	4
4.	ECD440	E-Vehicle Technology & Policy #	4	-	-	4
5.	ECD450	Industrial Electronics Practical	-	-	5	5
6.	ECD460	Communication Engineering Practical	-	-	4	4
7.	ECD470	Analog and Digital Electronics Practical	-	-	5	5
Extra &Co - Curricular Activities		Physical Education	-	2	-	2
		Library	-	1	-	1
		Total	18	3	14	35

 # Common with Mechanical Engineering

FIFTH SEMESTER

Sl.No	Course Code	Course	Hours Per Week			
			Theory Hours	Tutorial/ Drawing	Practical Hours	Total Hours
1.	ECD510	Analog and Digital Communication systems	5	-	-	5
2.	ECD520	Microcontroller and its Applications	5	-	-	5
3.	ECD531 ECD532 ECD533	Elective – I Theory 1. Very Large Scale Integration 2. Consumer Electronics 3. Basics of Digital Signal and Image Processing	4	-	-	4
4.	ECD540	Analog and Digital Communication Practical	-	-	5	5
5.	ECD550	Microcontroller Practical	-	-	4	4
6.	ECD561 ECD562 ECD563	Elective- I Practical 1. Very Large Scale Integration Practical 2. Consumer Electronics Practical 3. Signal and Image processing Practical	-	-	5	5
7.	ECD570	Entrepreneurship and Start –ups#	-	-	4	4
Extra &Co - Curricular Activities		Physical Education	-	2	-	2
		Library	-	1	-	1
		Total	14	3	18	35

 # Common with Mechanical Engineering

SIXTH SEMESTER

Sl.No	Course Code	Course	Hours Per Week			
			Theory Hours	Tutorial/ Drawing	Practical Hours	Total Hours
1.	ECD610	Computer Hardware Servicing and Networking	5	-	-	5
2.	ECD620	Biomedical Instrumentation	5	-	-	5
3.	ECD631 ECD632 ECD633	Elective – II Theory 1.Television Engineering 2. Mobile and Optical Communications 3. Embedded Systems	5	-	-	5
4.	ECD640	Computer Hardware Servicing and Networking Practical	-	-	6	6
5.	ECD651 ECD652 ECD653	Elective – II Practical 1.Television Engineering Practical 2. Mobile and Optical Communication Practical 3. Embedded Systems Practical	-	-	5	5
6.	ECD660	Project work and Internship	-	-	6	6
Extra &Co - Curricular Activities		Physical Education	-	2	-	2
		Library	-	1	-	1
		Total	15	3	17	35

ANNEXURE – II

SCHEME OF THE EXAMINATION

THIRD SEMESTER

Sl.No	Course Code	Course	EXAMINATION MARKS			Minimum for pass	Duration of Exam Hours
			Internal Assessment Marks	Auton-omous Exam Marks *	Total		
1.	ECD310	Electronic Devices and Circuits	25	75	100	40	3
2.	ECD320	Electrical Circuits and Instrumentation	25	75	100	40	3
3.	ECD330	Programming in 'C'	25	75	100	40	3
4.	ECD340	Electronic Devices and Circuits Practical	25	75	100	50	3
5.	ECD350	Electrical Circuits and Instrumentation Practical	25	75	100	50	3
6.	ECD360	Programming in 'C' Practical	25	75	100	50	3
7.	ECD370	Simulation Practical	25	75	100	50	3
TOTAL			**175**	**525**	**700**		

*** Examination will be conducted for 100 marks and it will be reduced to 75 marks.**

FOURTH SEMESTER

Sl.No	Course Code	Course	EXAMINATION MARKS			Minimum for pass	Duration of Exam Hours
			Internal assessment Marks	Auton-omous Exam Marks *	Total		
1.	ECD410	Industrial Electronics	25	75	100	40	3
2.	ECD420	Communication Engineering	25	75	100	40	3
3.	ECD430	Analog and Digital Electronics	25	75	100	40	3
4.	ECD440	E-Vehicle Technology & Policy #	25	75	100	40	3
5.	ECD450	Industrial Electronics Practical	25	75	100	50	3
6.	ECD460	Communication Engineering Practical	25	75	100	50	3
7.	ECD470	Analog and Digital Electronics Practical	25	75	100	50	3
TOTAL			**175**	**525**	**700**		

*** Examination will be conducted for 100 marks and it will be reduced to 75 marks.**

FIFTH SEMESTER

Sl.No	Course Code	Course	EXAMINATION MARKS			Minimum for pass	Duration of Exam Hours
			Internal assessment Marks	Autonomous Exam Marks *	Total		
1.	ECD510	Analog and Digital Communication systems	25	75	100	40	3
2.	ECD520	Microcontroller and its Applications	25	75	100	40	3
3.	ECD531 ECD532 ECD533	Elective - I-Theory 1. Very Large Scale Integration 2. Consumer Electronics 3. Basics of Digital Signal and Image Processing	25	75	100	40	3
4.	ECD540	Analog and Digital Communication Practical	25	75	100	50	3
5.	ECD550	Microcontroller Practical	25	75	100	50	3
6.	ECD561 ECD562 ECD563	Elective-I- Practical 1. Very Large Scale Integration Practical 2. Consumer Electronics Practical 3. Signal and Image processing Practical	25	75	100	50	3
7.	ECD570	Entrepreneurship and Start –ups	25	75	100	50	3
TOTAL			**175**	**525**	**700**		

*** Examination will be conducted for 100 marks and it will be reduced to 75 marks.**

SIXTH SEMESTER

Sl. No	Course Code	Course	EXAMINATION MARKS			Minimumfor pass	Duration of Exam Hours
			Internal assessment Marks	Autonomous Exam marks *	Total		
1.	ECD610	Computer Hardware Servicing and Networking	25	75	100	40	3
2.	ECD620	Biomedical Instrumentation	25	75	100	40	3
3.	ECD631 ECD632 ECD633	Elective – II-Theory 1.Television Engineering 2. Mobile and Optical Communications 3. Embedded Systems	25	75	100	40	3
4.	ECD640	Computer Hardware Servicing and Networking Practical	25	75	100	50	3
5.	ECD651 ECD652 ECD653	Elective –II- Practical 1.Television Engineering Practical 2. Mobile and Optical Communication Practical 3. Embedded Systems Practical	25	75	100	50	3
6.	ECD660	Project work and Internship	25	75	100	50	3
TOTAL			**150**	**450**	**600**		

***Examination will be conducted for 100 marks and it will be reduced to 75 marks.**

LIST OF EQUIVALENT COURSE FOR 'C' SCHEME TO 'D' SCHEME

THIRD SEMESTER

Sl.No	Code No	C Scheme	Code No	D Scheme
1	ECC310	Electronic Devices and Circuits	ECD310	Electronic Devices and Circuits
2	ECC320	Electrical Circuits and Instrumentation	ECD320	Electrical Circuits and Instrumentation
3	ECC330	Programming in 'C'	ECD330	Programming in 'C'
4	ECC340	Electronic Devices and Circuits Practical	ECD340	Electronic Devices and Circuits Practical
5	ECC350	Electrical Circuits and Instrumentation Practical	ECD350	Electrical Circuits and Instrumentation Practical
6	ECC360	Programming in 'C' Practical	ECD360	Programming in 'C' Practical
7	ECC370	Computer Application Practical for Electronics	D002	Computer Application Practical

FOURTH SEMESTER

Sl.No	Code No	C Scheme	Code No	D Scheme
1	ECC410	Industrial Electronics	ECD410	Industrial Electronics
2	ECC420	Communication Engineering	ECD420	Communication Engineering
3	ECC430	Digital Electronics	ECD430	Analog and Digital Electronics
4	ECC440	Linear Integrated Circuits	ECD430	Analog and Digital Electronics
5	ECC450	Industrial Electronics and Communication Engineering Practical	ECD450	Industrial Electronics Practical
6	ECC460	Integrated Circuits Practical	ECD470	Analog and Digital Electronics Practical
7	ECC470	Life and Employability Skills Practical	-	No Equivalent

FIFTH SEMESTER

Sl.No	Code No	C Scheme	Code No	D Scheme
1	ECC510	Advanced Communication Systems	ECD510	Analog and Digital Communication systems
2	ECC520	Microcontroller	ECD520	Microcontroller and its Applications
3	ECC530	Very Large Scale Integration	ECD531	Very Large Scale Integration
4	 ECC541 ECC542 ECC543	Elective – I-Theory 1. Digital Communication 2. Programmable Logic Controller 3. Bio Medical Instrumentation	 - - ECD620	 1.No Equivalent 2.No Equivalent 3.Bio Medical Instrumentation
5	ECC550	Advanced Communication Systems Practical	ECD540	Analog and Digital Communication Practical
6	ECC560	Microcontroller Practical	ECD550	Microcontroller Practical
7	ECC570	Very Large Scale Integration Practical	ECD561	Very Large Scale Integration Practical

SIXTH SEMESTER

Sl.No	Code No	C Scheme	Code No	D Scheme
1	ECC610	Embedded Systems	ECD633	Embedded Systems
2	ECC620	Computer Hardware Servicing and Networking	ECD610	Computer Hardware Servicing and Networking
3	 ECC631 ECC632 ECC633	Elective -II- Theory 1.Television Engineering 2. Test Engineering 3. Mobile Communication	 ECD631 - ECD632	Elective – II 1.Television Engineering 2. No Equivalent 3. Mobile and Optical Communication
4	ECC640	Embedded Systems Practical	ECD653	Embedded Systems Practical
5	ECC650	Computer Hardware Servicing and Networking Practical	ECD640	Computer Hardware Servicing and Networking Practical
6	ECC660	Advanced Microcontroller & Simulation Practical	-	No Equivalent
7	ECC670	Project Work	-	No Equivalent

ECD310 ELECTRONIC DEVICES AND CIRCUITS

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester: 16 weeks

Course	Instruction		Examination			
			Marks			
Electronic Devices and Circuits	**Hrs/ Week**	**Hrs/ Semester**	**Internal Assessment**	**Autonomous Examination**	**Total**	**Duration**
	5	80	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

TOPICS AND ALLOCATION OF HOURS:

UNIT	TOPICS	NO.OF HOURS
I	Filters, Zener diode and Opto-electronic devices	14
II	Bipolar Junction Transistor, Field Effect Transistor and UJT	15
III	Feedback, Amplifiers and Oscillators	15
IV	Special Semiconducting Devices(SCR, DIAC, TRIAC and MOSFET)	14
V	Wave shaping Circuits	13
	Tests and Model Exam	9
TOTAL		**80**

COURSE DESCRIPTION:

Every Electronics Engineer should have sound knowledge about the components used in Electronics Industry. This is vital in R&D Department for chip level troubleshooting. To meet the industrial needs, diploma holders must be taught about the most fundamental course, Electronic devices and Circuits. By studying this course, they will be skilled in handling all types of electronic devices and able to apply the skill in electronics system.

OBJECTIVES:

On completion of the following units of syllabus contents, the students must be able to:

- Know the importance of Filters.
- Know the construction, working principle and applications of Zener diode.
- Know the construction, working principle and applications of Opto electronic devices.
- Know the biasing methods of Transistors and their applications.
- Study the performance of special devices like UJT, FET.
- Study the Concept of Feedback, different types of Negative feedback connections.
- Know the Types of Transistor amplifiers ,Transistor oscillators and their applications.
- Study the performance of Special semiconducting devices like SCR, DIAC,TRIAC and MOSFET.
- Explain the concept of wave shaping circuits, Bistable Multivibrator and Schmitt trigger.
- Study the working principle of clippers, clampers, Voltage Multipliers and their applications.

COURSE OUTCOMES

Course	**ECD310 ELECTRONIC DEVICES AND CIRCUITS**
After successful completion of this course, the students should be able to	
D310.1	Understand the basic concepts of Filters, types and its applications, Zener diode construction, working principle, characteristics and its application and opto electronic devices, types, symbol, working, characteristics and applications.
D310.2	Know the transistor biasing in BJT, types, the operation and applications of transistor, FET and UJT construction, working principle, classification and application.
D310.3	Understand the basic concepts of feedback, oscillators and amplifiers, types, working principle and applications.
D310.4	Learn the construction, operation, characteristics and applications of SCR,DIAC,TRIAC& MOSFET.
D310.5	Understand the construction, operation, characteristics of wave shaping circuits such as clippers and clampers, voltage multipliers ,multivibrator and Schmitt trigger.

ECD310 ELECTRONIC DEVICES AND CIRCUITS

UNIT – I

FILTERS,ZENER DIODES AND OPTO-ELECTRONIC DEVICES **[14 Hrs]**

1.1 FILTERS

Definition - Types - Capacitor filter -Inductor filter [2 Hrs]

L section filter –Pi section and RC filter [2 Hrs]

Comparison and Applications of Filters [1 Hr]

1.2 ZENER DIODE

Construction, Working principle and Characteristics of Zener Diodes [3 Hrs]

Zener breakdown-Avalanche breakdown [1 Hr]

Zener diode as a Voltage regulator [1 Hr]

1.3OPTO-ELECTRONIC DEVICES

Definition - Types - Symbol, Working, Characteristics and Applications of LED, 7 Segment LED [2 Hrs]

Photo diode [1 Hr]

Phototransistor and Opto- coupler [1 Hr]

UNIT-II

BIPOLAR JUNCTION TRANSISTOR (BJT), FIELD EFFECT TRANSISTOR (FET), AND UNI JUNCTION TRANSISTOR (UJT) **[15 Hrs]**

2.1 BIPOLAR JUNCTION TRANSISTOR

Transistor biasing: Need for biasing [2 Hrs]

Types- Fixed bias, Collector to base bias and Self bias (Operation only, No derivation of circuit elements and parameters) [2 Hrs]

Define: Stability factor –Operation of Common Emitter Transistor as an Amplifier and as a switch [2 Hrs]

2.2 FIELD EFFECT TRANSISTOR (FET)

Construction – Working principle [2 Hrs]

Classification - Drain and Transfer Characteristics -Applications [1 Hr]

Comparison between FET and BJT [1 Hr]

- FET amplifier (common source amplifier). [1 Hr]

2.3. UNIJUNCTION TRANSISTOR (UJT)

Construction-Equivalent circuit-Operation-Characteristics-– [2 Hrs]

UJT as a relaxation oscillator [2 Hrs]

UNIT-III

FEEDBACK, AMPLIFIERS AND OSCILLATORS **[15 Hrs]**

3.1 FEEDBACK

Concept - effects of negative feedback- [2 Hrs]

Types of negative feedback connections – [2 Hrs]

-Applications [1 Hr]

3.2 AMPLIFIERS

Transistor amplifiers - Types – [2 Hrs]

RC coupled amplifier - Working and Frequency- response characteristics – [2 Hrs]

Working of Common Collector Amplifier (Emitter- follower) [2 Hrs]

3.3 OSCILLATORS

Transistor oscillators–Conditions for oscillation (Barkhausen criterion)- [1 Hr]

Classifications– Hartley Oscillator– [1 Hr]

Colpitts Oscillator – RC Phase shift oscillator [2 Hrs]

UNIT IV

SPECIAL SEMICONDUCTING DEVICES (SCR, DIAC,TRIAC AND MOSFET) **[14 Hrs]**

4.1 SCR (SILICON CONTROLLED RECTIFIER)

Symbol – Layered Structure – Transistor analogy - Working– [2 Hrs]

VI characteristics– Applications [1 Hr]

Comparison between SCR and Transistor [1 Hr]

4.2 DIAC(DIODE FOR ALTERNATING CURRENT)

Symbol –Layered structure - Working – [2 Hrs]

VI characteristics- Applications [1 Hr]

4.3 TRIAC(TRIODE FOR ALTERNATING CURRENT)

Symbol – Layered structure - Working – [2 Hrs]

VI characteristics- Applications [2 Hrs]

4.4 MOSFET

Types, Construction and Characteristics of N Channel MOSFET [2 Hrs]

and P channel MOSFET- Characteristics of enhancement and depletion mode MOSFET-

MOSFET as a switch [1 Hr]

UNIT -V

WAVE SHAPING CIRCUITS **[13 Hrs]**

5.1 CLIPPERS AND CLAMPERS

Construction and working of Positive, Negative and biased Clippers – [2 Hrs]

Construction and working of Positive and Negative Clamper [3 Hrs]

5.2 VOLTAGE MULTIPLIERS

Construction and working of Voltage Doubler [2 Hrs]

and Tripler [1 Hr]

5.3 MULTIVIBRATOR AND SCHMITT TRIGGER

Construction – Working – [2 Hrs]

Waveform of Astable and Monostable Multivibrator using Transistor [2 Hrs]

and Schmitt Trigger using Transistors [1 Hr]

Tests & Model Exam **[9 Hrs]**

TEXT BOOKS:

S.NO	TITLE	AUTHOR	PUBLISHER WITH EDITION
1.	Electronic Devices and Circuits	Sallaivahanan, N.Suresh Kumar, A.Vallavaraj	Tata McGraw Publication 3rd Edition 2016
2.	Electronics Devices and circuit theory	Boyestad&Nashelsky	PHI , New Delhi 2009

REFERENCE BOOKS:

S.NO	TITLE	AUTHOR	PUBLISHER WITH EDITION
1.	Electronic Principles	Malvino	Tata McGraw Hill Publication 2010
2.	Electronics Devices & Circuits	Allen Mottershed	PHI, 2009
3.	Electronics Devices & Circuits	Jacob Millman and Halkias	Tata McGraw – Hill publication 3rd Edition 2010
4.	Optical Fiber Communication	GerdKeiser	Tata McGraw – Hill Publication 5th Edition 2013

LEARNING WEBSITES

1.https://www.electronics-tutorials.ws/
2.http://www.learnabout-electronics.org/
3.https://www.jntua.ac.in/gate-online-classes/registration/downloads/material/a159282103576.pdf
4 .https://www.pdfdrive.com/semiconductor-devices-e188099997.html
5.https://www.seeedstudio.com/blog/2017/02/24/electronic-websites/

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	-	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
D310.1	3	3	3	3	2	2	3	3	2	2
D310.2	3	3	3	3	2	2	3	3	2	2
D310.3	3	3	3	3	2	2	3	3	2	2
D310.4	3	3	3	3	2	2	3	3	2	2
D310.5	3	3	3	3	2	2	3	3	2	2
D310 Total	15	15	15	15	10	10	15	15	10	10
Correlation Level	3	3	3	3	2	2	3	3	2	2

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD320 ELECTRICAL CIRCUITS AND INSTRUMENTATION

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 16 weeks

Course	Instruction		Examination			
			Marks			
Electrical Circuits and Instrumentation	**Hrs/ Week**	**Hrs/ Semester**	**Internal Assessment**	**Autonomous Examination**	**Total**	**Duration**
	6	96	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

TOPICS AND ALLOCATION:

UNIT	TOPICS	NO.OF HOURS
I	DC Circuits and Theorems	17
II	AC Circuits	17
III	Electrical Machines	17
IV	Transducers and CRO	18
V	Measurement and Instruments	18
	Test& Model Exam	9
TOTAL		96

COURSE DESCRIPTION:

This course enables the students with concepts of DC circuits & network theorems, AC circuits. The subject also deals with principles and working of different Measuring instruments and Electrical Machines. The introduction of this subject imparts the knowledge for students to analyze the electrical circuits.

OBJECTIVES:

On successful completion of the course, the students must be able to

- State Ohm's law and Kirchoff's laws.
- Understand the DC circuit and network theorems.
- Understand series and parallel circuits.
- Define various terms related to AC circuits.
- Get knowledge on AC circuits.
- Understand about resonance in series and parallel circuits.

- Know the operation of different Electrical machines.
- Know the operation of measuring instruments.
- Have basic knowledge on circuit analysis.

COURSE OUTCOMES

Course	**ECD 320 ELECTRICAL CIRCUITS AND INSTRUMENTATION**
After successful completion of this course, the students should be able to	
D320.1	Apply Electrical laws to solve D.C. circuits and network theorems for finding electrical parameters of D.C circuits.
D320.2	Analyze Basics of A.C. circuits, series and parallel RL, RC, RLC circuits and series and parallel resonance circuits.
D320.3	Understand the construction, working principle, EMF Equation, Losses, efficiency, test and applications of Transformer, supply, DC generator and various electric motors.
D320.4	Understand the operation, construction and applications of different types of transducers, Cathode Ray Oscilloscope (CRO),Digital Storage Oscilloscope (DSO) and Function generator.
D320.5	Understand the construction and operation of different types of measuring instruments and the basics about measurement.

ECD320 ELECTRICAL CIRCUITS AND INSTRUMENTATION

UNIT I

D.C.CIRCUITS AND THEOREMS **[17 Hrs]**

1.1 DEFINITION AND UNIT

Voltage, current, power, resistance and conductance. [2 Hrs]

1.2 ELECTRICAL LAWS

Ohm's law – Simple problems in Ohm's law – [2 Hrs]

Kirchoff's current law and Kirchoff's voltage law.– [2 Hrs]

1.3 BASIC DC CIRCUITS

Series and Parallel connections of resistors — [2 Hrs]

Voltage and Current division in series and parallel circuits – [2 Hrs]

Mesh analysis for DC circuits (simple problems).– [1 Hr]

1.4 NETWORK THEOREMS

Thevenin's Theorem–Superposition theorem— [3 Hrs]

Maximum power transfer theorem – (Statement, Explanation, Simple problems). [3 Hrs]

UNIT II

A.C CIRCUITS **[17 Hrs]**

2.1 BASIC AC CIRCUITS

Definition for impedance, reactance, admittance

And power factor– [2 Hrs]

Sinusoidal and Non sinusoidal waveforms- Average and RMS value [1 Hr]

Current and Voltage relationship in R, L and C circuits – [2 Hrs]

Analysis of RL, RC and RLC series circuits – [2 Hrs]

Analysis of RL, RC and RLC parallel circuits (simple problems). [2 Hrs]

2.2 RESONANCE

Series resonance – Parallel resonance – [3 Hrs]

Condition for resonance–frequency response – [3 Hrs]

Resonant frequency, Q factor and bandwidth. [2 Hrs]

UNTI III

ELECTRICAL MACHINES **[17 Hrs]**

3.1 TRANSFORMER

Construction – working principle – EMF equation – Losses in transformer [2 Hrs]

–efficiency of a transformer – OC, SC test on transformer– [2 Hrs]

Applications of transformer – [1 Hr]

3.2 SINGLE PHASE AND THREE PHASE SUPPLY

Introduction to single phase and three phase supply– [2 Hrs]

– Star Delta transformation – [1 Hr]

Difference between single phase and three phase supply– [1 Hr]

3.3 DC GENERATOR

Construction, working principle – [2 Hrs]

EMF equation – [1 Hr]

3.4 ELECTRIC MOTORS

DC motor –Single phase induction motor — [2 Hrs]

Three phase induction motor – Capacitor start induction motor – [2 Hrs]

–stepper- motor – Universal Motors [1 Hr]

UNIT IV

TRANSDUCERS & CRO **[18 Hrs]**

4.1 TRANSDUCERS

Classification of Transducers – Strain gauge: Principle of operation – [2 Hrs]

construction, types, advantage, disadvantage and application – [2 Hrs]

Advantage of semiconductor strain gauge over metallic strain gauge — [1 Hr]

Photo electric transducer – [1 Hr]

LVDT [1 Hr]

RVDT [1 Hr]

Load cell. [1 Hr]

4.2 CRO

CRT – Block diagram and operation of CRO [2 Hrs]

Applications of CRO Dual trace [2 Hrs]

Digital Storage Oscilloscope

Block diagram, working principle [2 Hrs]

Function Generator

Block Diagram, Working principle [3 Hrs]

UNIT V

MEASUREMENT AND INSTRUMENTS [18 Hrs]

5.1 DEFINITION

Definition for Measurement, Accuracy, precision, resolution, Calibration. [2 Hrs]

5.2 INSTRUMENTS

Operation of Thermo couple– [1 Hr]

working principle of Thermistor – [1 Hr]

PMMC Instrument: Construction and working principle– [2 Hrs]

Moving Iron Instrument: Construction and working principle – [2 Hrs]

Shunts and Multipliers – Potentiometer – [1 Hr]

DC ammeter – DC voltmeter – Voltmeter Sensitivity [1 Hr]

5.3 MEASUREMENT

Errors in Measurement – [1 Hr]

Temperature measurement using thermocouple [2 Hrs]

Temperature measurement using Thermistors– [2 Hrs]

Resistance measurement Wheatstone bridge– [1 Hr]

Measurement of Inductance: Maxwell's bridge [1 Hr]

–Measurement of Capacitance: Schering Bridge [1 Hr]

Tests & Model Exam [9 Hrs]

TEXT BOOKS:

S.No	Title	Author	Publisher with edition
1.	Electrical Technology	B.L.Theraja ,A.K.Theraja	S. Chand & co publisher, New Delhi 2005
2.	Electronic Measurements and Instrumentation	R.K.Rajput	S. Chand (Third Edition)-2008

REFERENCE BOOKS:

S.No	Title	Author	Publisher with edition
1.	Electric Circuit Theory	Dr.M.Arumugam, N.Premkumaran	Khanna Publishers, New Delhi, 5th edition1979.
2.	A Course in Electrical and Electronic Measurements and Instrumentation	A.K.Sawhney &	Dhanpat raj &co (P) Limited 1993.

LEARNING WEBSITES

1.https://www.allaboutcircuits.com/textbook/

2. https://www.physics.wisc.edu/courses/home/fall2020/321/Lab%20Instructions/lab02-2020.pdf

3.https://www.pdfdrive.com/electricalelectronic-instrumentation-i-e18436280.html

4.http://www.freebookcentre.net/electronics-ebooks-download/Communication-Systems-by-Dr-Cong-Ling.html

5. https://engineeringbookspdf.com/instrumentation-and-measurement-in-electrical-engineering-pdf-free-download/1726

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
D320.1	3	3	3	2	2	2	2	3	2	2
D320.2	3	3	3	2	2	2	2	3	2	2
D320.3	3	3	3	2	2	2	2	3	2	2
D320.4	3	3	3	2	2	2	2	3	2	2
D320.5	3	3	3	2	2	2	2	3	2	2
D320 Total	15	15	15	10	10	10	10	15	10	10
Correlation Level	3	3	3	2	2	2	2	3	2	2

Correlation level 1- Slight (low)
Correlation level 2- Moderate (Medium)
Correlation level 3- Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD330 PROGRAMMING IN 'C'

TEACHING AND SCHEME OF EXAMINATION:

No. of weeks per semester: 16 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/ Week	Hrs / Semester	Internal Assessment	Autonomous Examination	Total	
Programming in 'C'	5	80	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

TOPICS AND ALLOCATION OF HOURS:

UNIT	TOPICS	NO.OF HOURS
I	Basics of 'C'	14
II	C operators, decision making, branching and Looping statements	14
III	Arrays and strings	14
IV	Structure and union	15
V	Functions &files I/O	14
	Tests & model exam	9
TOTAL		**80**

COURSE DESCRIPTION:

'C' language is the most widely used computer language, which is being taught as a core course. C is the general purpose high level language. Due to the flexibility, it is suitable for different development environments. 'C' language has importance and popularity in recently developed and advanced software industry. 'C' language can also be used for system level programming and it is still considered as first priority programming language. This course covers the basic concepts of 'C'.

OBJECTIVES:

The course aims to provide exposure/train the students to do programming in C. At the end of the Course, the students will be able to

- Know the basics of C.
- Write algorithm and flow chart for any problems.
- Know operators used in 'C' and Decision making statements.
- Define and understand about arrays and functions.

- Define and understand about structure and union.
- Understand strings, string handling functions.
- Develop programs using C operators, decision making statements.
- Develop programs using arrays, function, and structure.
- Understand Input/ Output Operations on files, Error handling during I/O operations and Random Access to files

COURSE OUTCOMES

Course	**ECD330 PROGRAMMING IN 'C'**
After successful completion of this course, the students should be able to	
D330.1	Understand the fundamentals of C programming and I/O statements.
D330.2	Apply C operators, Decision making, branching and looping statements to write C programs.
D330.3	Understand about arrays and strings to develop the program.
D330.4	Understand about structures and unions to write C programs.
D330.5	Know about function and C files I/O.

ECD330 PROGRAMMING IN 'C'

UNIT I

BASICS OF C **[14 Hrs]**

1.1 INTRODUCTION TO C

History of 'C' – Structure of C program – Steps for execution of C program – [1 Hr]

Functions performed by Compiler, Linker – Algorithm & flow chart – [1 Hr]

Low level and High level Programming language – [1 Hr]

C character set –Tokens –Constants – Key words – [2 Hrs]

Variables –Data types – Declaration of Variables – [2 Hrs]

Assigning Values to variables. [1 Hr]

1.2 I/O STATEMENTS

Formatted input [2 Hrs]

Formatted output [2 Hrs]

Unformatted I/O statements. [2 Hrs]

UNIT II

C OPERATORS, DECISIONMAKING,BRANCHING AND LOOPING STATEMENTS **[14 Hrs]**

2.1 C OPERATORS

Arithmetic, Logical, Assignment, Relational, Increment, Decrement, [2 Hrs]

Conditional, Bitwise and Special operators – [2 Hrs]

Precedence and Associativity – [2 Hrs]

C expressions: Arithmetic expressions, Evaluation of expressions. [1 Hr]

2.2 DECISION MAKING,BRANCHING AND LOOPING STATEMENTS

Simple if statement, if- else, else - if ladder and nested if-else statement [2 Hrs]

– switch statement – while, do-while statements – [1 Hr]

for loop, go to, break & continue statement – [1 Hr]

Program to find whether the given number is even or odd – [1 Hr]

Program to perform the Arithmetic operations using switch statement– [1 Hr]

Program to find sum of series using "while" loop. [1 Hr]

UNIT III

ARRAYS AND STRINGS **[14 Hrs]**

3.1 ARRAYS

Definition of array– [1 Hr]

Declaration and initialization of One dimensional, [2 Hrs]

Two dimensional arrays – [1 Hr]

Accessing array elements –Program to find sum of the elements of array – [2 Hrs]

Program for matrix addition. [2 Hrs]

3.2 STRINGS

Declaration and initialization of string variables, [2 Hrs]

String handling Functions: strlen (), strcpy() , strcat(), strcmp() – [2 Hrs]

Program to sort the set of strings using string handling functions [2 Hrs]

UNIT IV

STRUCTURE AND UNION **[15 Hrs]**

4.1 STRUCTURE

Structure: Definition of structure – Need of structure – [2 Hrs]

Defining and initializing structure –Arrays of structures, [2 Hrs]

Arrays within structures, structures within structures– [2 Hrs]

Program to prepare the total marks for N students

by reading the Name, Reg. No, Marks 1 to Marks 5 using array of structure. [2 Hrs]

4.2 UNION

Declaring and Initializing unions – [2 Hrs]

Program to declare, initialize an UNION– [3 Hrs]

Advantages of unions– [1 Hr]

Difference between Union and structure. [1 Hr]

UNIT V

FUNCTION AND C FILES I/O **[14 Hrs]**

5.1 FUNCTION

Types – In built functions – [1 Hr]

User defined functions – Function definition – [2 Hrs]

Function call: call by value – [2 Hrs]

Program to find factorial of given N numbers using function– [1 Hr]

Program to count the number of digits in a number using function. [1 Hr]

5.2 C FILES I/O

Opening, Reading, Writing and closing a file – [2 Hrs]

Program using file [1 Hr]

Input/ Output Operations on files, [1 Hr]

Error handling during I/O operations, [2 Hrs]

Random Access to files [1 Hr]

Tests & Model Exam [9 Hrs]

TEXT BOOKS:

S.No	Title	Author	Publisher with Edition
1.	Programming in ANSI C	E.Balaguruswamy	Tata Mc –GrawHill, New Delhi, Third Edition,2010
2.	Introduction to Computer Graphics	N. Krishnamoorthy	Tata Mc –GrawHill, New Delhi, Second Edition,2009
3.	A Text Book on C	E.Karthikeyan	PHI Private Limited, New Delhi , 2008

REFERENCE BOOKS:

S.No	Title	Author	Publisher with Edition
1.	Programming and Problem solving using C	ISRD Group, Lucknow	Tata Mc- GrawHill, New Delhi, Sixth Reprint , 2010
2.	Let us C	Yeswanth, Kanetkar	BPB Publications , Fourth Revised Edition, 2007
3.	Programming in C	D.Ravichandran	New Age International Publishers, C, FirstEdition1996, Reprint2011
4.	Computer Concepts And Programming in C	Dr.S.S.Khandare	S.Chand & Company Ltd. New Delhi, First Edition 2010
5.	Complete Knowledge in C	Sukhendu Dey, Debobrata Dutta	Narosa Publishing House, New Delhi, Reprint2010
6.	Programming in C	ReemaTheraja	Oxford University Press, First Edition, 2011
7.	Practical C Programming	Steve Oualline	O'Reilly, Shroff Publishers, Eleventh Indian Reprint, Oct2010

LEARNING WEBSITES

1. https://www.tutorialspoint.com/ansi_c/c_introduction.htm
2. https://www.youtube.com/watch?v=8PopR3x-VMY
3. https://www.youtube.com/watch?v=si-KFFOW2gw
4. https://www.guru99.com/c-programming-language.html
5. https://www.cprogramming.com/tutorial/c/lesson1.html

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	-	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
D330.1	3	3	3	3	2	2	2	3	2	3
D330.2	3	3	3	3	2	2	2	3	2	3
D330.3	3	3	3	3	2	2	2	3	2	3
D330.4	3	3	3	3	2	2	2	3	2	3
D330.5	3	3	3	3	2	2	2	3	2	3
D330 Total	15	15	15	15	10	10	10	15	10	15
Correlation Level	3	3	3	3	2	2	2	3	2	3

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD340 ELECTRONIC DEVICES AND CIRCUITS PRACTICAL

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester: 16 Weeks

Course	Instruction		Examination			
Electric Devices and Circuits Practical	Hrs/ Week	Hrs/ Semester	Marks			Duration
	4	64	Internal Assessment	Autonomous Examination	Total	
			25	100*	100	3Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

DETAILED ALLOCATION OF MARKS

S.No	DESCRIPTION	MARKS
1.	CIRCUIT DIAGRAM	25
2.	CONNECTION	25
3.	EXECUTION & HANDLING OF EQUIPMENT	25
4.	OUTPUT /RESULT	10
5.	VIVA–VOCE	5
6.	MINI PROJECT	10
TOTAL		**100**

Mini Project Evaluation (10 marks)

Breakup Details

1	Project Description	05
2	Project Demo	05
	Total	**10**

COURSE DESCRIPTION:

Every Electronics Engineer should have sound knowledge about the components used in Electronics Industry. This is vital in R &D Department for chip level troubleshooting. To meet the industrial needs, diploma holders must be taught about the most fundamental subject, Electronic devices and Circuits Practical. By doing practical experience in this, they will be skilled in handling all types of electronic circuits and able to apply the skill in electronic systems.

EQUIPMENTS REQUIRED: (FOR A BATCH OF 30 STUDENTS)

S.No	Name of the Equipments	Range	Required Nos.
1	DC Regulated Power supply	0-30V,1A	10
2	DC High Voltage Power Supply	0-250V,1A	2
3	Signal Generator	1MHz	4
4	Dual trace CRO	20MHz/ 30MHz	5
5	Digital Multimeter	-	10
6	DC Voltmeter(Analog/Digital)	Different Ranges	15
7	DC Ammeter(Analog/Digital)	Different Ranges	15

OBJECTIVES:

On completion of the following experiments, the students must be able to

1) Know the Cold Checking of Active and Passive Components.
2) Find out the Unknown Resistance value of a Resistor using Colour Coding.
3) Find out the Unknown Capacitance value of a Capacitor using Colour Coding.
4) Find out the Unknown Inductance value of an Inductor using Colour Coding.
5) Understand the concept, working principle and applications of PN Junction diode.
6) Understand the concept, working principle and applications of Zener diode.
7) Understand the concept, working principle and applications of BJT and FET.
8) Understand the concept, working principle and applications of UJT.
9) Understand the concept, working principle and applications of SCR.
10) Understand the concept, working principle and applications of DIAC and TRIAC.
11) Understand the concept, working principle and applications of Clippers and Clampers.
12) Understand the concept, working principle and applications of various types of Negative feedback amplifiers.
13) Understand the concept, working principle and applications of Astable Multivibrator.
14) Construct a circuit to glow the different color LED alternatively.
15) Develop the Mini Projects.

COURSE OUTCOME:

Course	**ECD340 ELECTRONIC DEVICES AND CIRCUITS PRACTICAL**
After successful completion of this course, the students should be able to	
D340.1	Construct and test the characteristics of PN junction diode and Zener diode
D340.2	Construct and observe the waveforms of Full wave (centre tapped) rectifier, full wave (Bridge) Rectifier with and without filters.
D340.3	Construct and test the characteristics of Common Emitter Transistor, Common Source Field Effect Transistor, Uni Junction Transistor (UJT) and V-I characteristics of switching devices. (SCR, TRIAC, DIAC).
D340.4	Construct and Test the characteristics of Common Emitter amplifier and switching characteristics of Astable Multivibrator
D340.5	Construct the circuit for glowing LED and develop the mini projects with report.

ECD340 ELECTRONIC DEVICES AND CIRCUITS PRACTICAL

Note: At least 5 experiments should be constructed using breadboard/soldering

List of experiments to be conducted

1. Construct a circuit to test the forward and reverse bias characteristics of a PN Junction Silicon diode. Find the value of its cut-in voltage.
2. Construct a circuit to test the forward and reverse bias characteristics of a Zener diode. Find the value of its reverse break down voltage.
3. Construct a Full wave (center tapped) rectifier and test its input and output waveforms with and without Capacitor filter. Find its maximum voltage.
4. Construct a Full wave (Bridge) rectifier and test its input and output waveforms with and without Capacitor filter. Find its maximum voltage.
5. Construct a Common Emitter Transistor circuit and test its input and output characteristic curves.
6. Construct a Common Source Field Effect Transistor circuit and test its drain and transfer characteristic curves.
7. Construct a circuit to test the Turning on and Turning off characteristics of SCR and find out the forward break over voltage, the value of Latching and Holding currents.
8. Construct a circuit to test the bidirectional characteristics of DIAC and plot its switching characteristics.
9. Construct a circuit to test the bidirectional characteristics of TRIAC and plot its switching characteristics.
10. Construct a Common emitter amplifier circuit and test its frequency response characteristics with and without Current series feedback introduced in it.
11. Construct a circuit to test the switching characteristics of Astable Multivibrator.
12. Construct a circuit to test negative resistance characteristics of UJT .
13. Construct a circuit to glow the different color LED alternatively.
14. Mini Project.

    The mini project is activity based and it may be given to group of maximum of six students for hands on experience and to create scientific temper.

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:

a) Attendance (Award of marks same as theory courses)	:	05 Marks
b) Procedure/ observation and tabulation/ Other Practical related Work	:	05 Marks
c)Tests	:	10 Marks
d) Student Centered Learning (SCL) work sheet	:	05 Marks
Total		25 Marks

LEARNING WEBSITES

1. http://vlabs.iitb.ac.in/vlab/electrical/index.html
2. https://www.industrial-electronics.com/experiments_0.html
3. http://vlabs.iitkgp.ernet.in/be/
4. http://www2.ece.ohio-state.edu/ee327/
5. https://www.objectivebooks.com/2016/11/edc-lab-viva-questions-and-answers.html

CO- POs & PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
D340.1	3	3	3	3	3	3	3	3	2	3
D340.2	3	3	3	3	3	3	3	3	2	3
D340.3	3	3	3	3	3	3	3	3	2	3
D340.4	3	3	3	3	3	3	3	3	2	3
D340.5	3	3	3	3	3	3	3	3	2	3
Total	15	15	15	15	15	15	15	15	10	15
Correlation Level	3	3	3	3	3	3	3	3	2	3

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

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ECD340 ELECTRONIC DEVICES AND CIRCUITS PRACTICAL

MODEL QUESTION PAPER

Note: At least 5 experiments should be done using Soldering board / Bread board

S.No	Experiments	CO	PO
1	Construct a circuit to test the forward and reverse bias characteristics of a PN Junction Silicon diode. Find the value of its cut-in voltage.	D340.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
2	Construct a circuit to test the forward and reverse bias characteristics of a Zener diode. Find the value of its reverse break down voltage.	D340.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
3	Construct a Full wave (center tapped) rectifier and test its input and output waveforms with and without Capacitor filter. Find its maximum voltage.	D340.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
4	Construct a Full wave (Bridge) rectifier and test its input and output waveforms with and without Capacitor filter. Find its maximum voltage.	D340.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
5	Construct a Common Emitter Transistor circuit and test its input and output characteristic curves.	D340.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
6	Construct a Common Source Field Effect Transistor circuit and test its drain and transfer characteristic curves.	D340.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
7	Construct a circuit to test the Turning on and Turning off characteristics of SCR and find out the forward break over voltage, the value of Latching and Holding currents.	D340.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
8	Construct a circuit to test the bidirectional characteristics of DIAC and plot its switching characteristics.	D340.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
9	Construct a circuit to test the bidirectional characteristics of TRIAC and plot its switching characteristics.	D340.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
10	Construct a Common emitter amplifier circuit and test its frequency response characteristics with and without Current series feedback introduced in it.	D340.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
11	Construct a circuit to test the switching characteristics of Astable Multivibrator.	D340.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
12	Construct a circuit to test negative resistance characteristics of UJT	D340.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
13	Construct a circuit to glow the different color LED alternatively.	D340.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
14.	**Mini Project**	**D340.5**	**PO1,PO2,PO3,PO4, PO5,PO6,PO7**

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ECD350 ELECTRICAL CIRCUITS AND INSTRUMENTATION PRACTICAL

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester: 16 Weeks

Course	Instruction		Examination			
Electrical Circuits and Instrumentation Practical	Hrs/ Week	Hrs/ Semester	Marks			Duration
	4	64	Internal Assessment	Autonomous Examination	Total	
			25	100*	100	3Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

DETAILED ALLOCATION OF MARKS

S.No	DESCRIPTION	MARKS
1	CIRCUIT DIAGRAM	25
2	CONNECTION	25
3	EXECUTION & HANDLING OF EQUIPMENT	25
4	OUTPUT /RESULT	10
5	VIVA–VOCE	5
6	MINI PROJECT	10
TOTAL		**100**

Mini Project Evaluation (10 marks)

Breakup Details

1	Project Description	05
2	Project Demo	05
Total		**10**

COURSE DESCRIPTION:

This course enables the students with concepts of DC circuits & network theorems, AC circuits. The course also deals with principles and working of different Measuring instruments and Electrical Machines .The introduction of this subject impart the knowledge for students to analyze the electrical circuits.

EQUIPMENTS REQUIRED: (FOR A BATCH OF 30 STUDENTS)

S.No	Name of the Equipments	Range	Required Nos
1.	DC regulated power supply	(0-30V),1A	8
2.	Signal generators	1MHz	3
3.	CRO	20MHz	4
4.	DC Voltmeter	(0-15V)	8
5.	DC Ammeter	(0-300μA)	6
6.	DC Ammeter	(0-100mA)	8
7.	Digital Multimeter	-	4
8.	Galvanometer	-	1
9.	Decade Resistance Box	-	1

OBJECTIVES:

On completion of all the experiments, the students must be able to

- Verify Ohm's law.
- Verify Kirchoff's laws.
- Verify network theorems.
- Test the performance of electric circuit.
- Determine the characteristics of measuring instruments.
- Use CRO.
- Construct and test the charger for cell Phone.
- Develop the Mini Projects.

COURSE OUTCOMES

Course	**ECD350 ELECTRICAL CIRCUITS AND INSTRUMENTATION PRACTICAL**
After successful completion of this course, the students should be able to	
D350.1	Construct and analyze circuits using Ohm's law, Kirchoff's laws, network theorems (Superposition Theorem, Thevenin's theorem and maximum power transfer theorem).
D350.2	Construct and analyze resonance circuits and calibrate the voltmeter and ammeter.
D350.3	Construct and determine the unknown resistance value using wheat stone bridge and measure the amplitude and frequency of the signal using CRO.
D350.4	Construct and understand the performance of various transducers. (Thermistor, LVDT and Strain Gauge).
D350.5	Construct Charger for cell phone and develop the mini projects with report.

ECD350 ELECTRICAL CIRCUITS AND INSTRUMENTATION PRACTICAL

Note: Atleast 9 experiments should be constructed using breadboard

1. Construct a circuit to verify Ohm's law.
2. Construct a circuit to verify Kirchoff's voltage and current law.
3. Construct a circuit to verify Superposition theorem.
4. Construct a circuit to verify Thevenin's Theorem.
5. Construct a circuit to verify Maximum power transfer Theorem.
6. Construct and test the performance of series resonant circuit.
7. Calibrate the given ammeter and voltmeter.
8. Construct and test the performance of Wheatstone bridge.
9. Measure the amplitude and frequency of signals using CRO.
10. Test the performance of LVDT.
11. Measure strain using strain gauge.
12. Determine the characteristics of a thermistor.
13. Construct and test the charger for cell Phone.
14. Mini Project.

The mini project is activity based and it may be given to group of maximum of six students for hands on experience and to create scientific temper

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:

a) Attendance (Award of marks same as theory courses)	:	05 Marks
b) Procedure/ observation and tabulation/ Other Practical related Work	:	05 Marks
c)Tests	:	10 Marks
d) Student Centered Learning (SCL) work sheet	:	05 Marks
Total		25 Marks

LEARNING WEBSITES

1.https://vlab.amrita.edu/?sub=1&brch=75
2.https://www.electronicshub.org/electronics-mini-project-circuits/
3.http://vlabs.iitkgp.ac.in/asnm/
4.https://www.pdfdrive.com/basic-electrical-engineering-e161605270.html
5.https://webstor.srmist.edu.in/web_assets/downloads/2021/15EE103L-electric-circuits-lab.pdf

CO- POs & PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
D350.1	3	3	3	3	3	3	3	3	2	3
D350.2	3	3	3	3	3	3	3	3	2	3
D350.3	3	3	3	3	3	3	3	3	2	3
D350.4	3	3	3	3	3	3	3	3	2	3
D350.5	3	3	3	3	3	3	3	3	2	3
D350 Total	15	15	15	15	15	15	15	15	10	15
Correlation Level	3	3	3	3	3	3	3	3	2	3

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

ECD350 ELECTRICAL CIRCUITS AND INSTRUMENTATION PRACTICAL

MODEL QUESTION PAPER

S.No	Experiments	CO	PO
1	Construct a circuit to verify Ohm's law.	D350.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
2	Construct a circuit to verify Kirchoff's voltage and current law.	D350.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
3	Construct a circuit to verify Superposition theorem.	D350.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
4	Construct a circuit to verify Thevenin's Theorem.	D350.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
5	Construct a circuit to verify Maximum power transfer Theorem.	D350.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
6	Construct and test the performance of series resonant circuit.	D350.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
7	Calibrate the given ammeter and voltmeter.	D350.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
8	Construct and test the performance of Wheatstone bridge.	D350.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
9	Measure the amplitude and frequency of signals using CRO.	D350.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
10	Test the performance of LVDT.	D350.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
11	Measure strain using strain gauge.	D350.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
12	Determine the characteristics of a thermistor.	D350.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
13	Construct and test the charger for cell Phone.	D350.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
14.	**Mini Project**	**D340.5**	**PO1,PO2,PO3,PO4, PO5,PO6,PO7**

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ECD360 PROGRAMMING IN 'C' PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

No. of weeks per semester: 16 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/Week	Hrs / Semester	Internal Assessment	Autonomous Examination	Total	
Programming in 'C' Practical	4	64	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

DETAILED ALLOCATION OF MARKS

S.NO	DESCRIPTION	MARKS
1.	ALGORITHM /FLOWCHART	25
2.	PROGRAM	25
3.	EXECUTING PROGRAM	25
4.	OUTPUT /RESULT	10
5.	VIVA–VOCE	5
6.	MINI PROJECT	10
TOTAL		**100**

Mini Project Evaluation (10 marks)

Breakup Details

1	Project Description	05
2	Project Demo	05
	Total	**10**

COURSE DESCRIPTION:

To provide the platform for software

HARDWARE REQUIRMENT: (FOR A BATCH OF 30 STUDENTS)

Desktop/laptop computers: 30 nos

Laser Printer: 01 no

SOFTWARE REQUIREMENT:

C-compiler and editor

OBJECTIVES:

At the end of the Course, the students will be able to

- Think the logic to solve the given problem.
- Know the concepts of constants, variables, data types and Operators.
- Develop programs to evaluate expression by knowing 'C' precedence rule.
- Write programs using different decision making, looping statements.
- Write programs using arrays, function and structure.
- Develop a program to print the college name 10 times.
- Develop the Mini Projects.

COURSE OUTCOMES

Course	**ECD360 PROGRAMMING IN 'C' PRACTICAL**
After successful completion of this course, the students should be able to	
D360.1	Write C programs to calculate simple interest ,compound interest and find the solutions for quadratic equation
D360.2	Develop C programs to find the odd and even number ,sum of series and perform arithmetic operations.
D360.3	Write C programs to find the biggest number among three numbers, print the Fibonacci series and find the factorial of given numbers, prepare the total marks of N students and swap the values of two variables.
D360.4	Write C programs to calculate sum and average of three numbers, sort the names and count the number of digits.
D360.5	Write C programs to perform the matrix addition, print the multiplication table, print the college name and develop the mini projects with report.

ECD360 PROGRAMMING IN 'C' PRACTICAL

1. Write C program to calculate simple interest and compound interest.
2. Write C program to find the solution of a quadratic equation.
3. Write C program to find whether the given number is even or odd.
4. Write C program to find the sum of series using 'While' loop.
5. Write C program to perform the Arithmetic operation based on numeric key press using switch case statement.
   (1-Addition,2-Subtraction,3–multiplication,4- Division).
6. Write C program to find the biggest number among three numbers.
7. Write C program to print Fibonacci series.
8. Write C program to find factorial of given Numbers using function.
9. WriteCprogramtopreparethetotalmarksforNstudentsbyreadingtheName,Reg.No,Marks1 toMarks6 using array of structure.
10. Write C program to swap the values of two variables.
11. Write C program to calculate the sum and average of given three numbers using function.
12. Write C program to sort the names in alphabetical order.
13. Write C program to count the number of digits in a given integer and print the reverse number.
14. Write C program for matrix addition.
15. Write C program to print multiplication table.
16. Write C program to print the college name 10 times.
17. Mini Project

    The mini project is activity based and it may be given to group of maximum of six students for hands on experience and to create scientific temper

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:

a) Attendance (Award of marks same as theory courses)	:	05 Marks
b) Procedure/ observation and tabulation/ Other Practical related Work	:	05 Marks
c)Tests	:	10 Marks
d) Student Centered Learning (SCL) work sheet	:	05 Marks
Total		25 Marks

LEARNING WEBSITES

1. https://www.learn-c.org/
2. https://www.includehelp.com/articles/top-5-websites-for-learning-c-programming-language.aspx
3. https://www.w3resource.com/c-programming-exercises/
4. https://youtu.be/iY1gg0ftp84
5. https://youtu.be/72fIizW3N-8

CO- POs & PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
D360.1	2	2	3	3	3	3	3	2	3	3
D360.2	2	2	3	3	3	3	3	2	3	3
D360.3	2	2	3	3	3	3	3	2	3	3
D360.4	2	2	3	3	3	3	3	2	3	3
D360.5	2	2	3	3	3	3	3	2	3	3
D360 Total	10	10	15	15	15	15	15	10	15	15
Correlation Level	2	2	3	3	3	3	3	2	3	3

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

ECD 360 PROGRAMMING IN 'C' PRACTICAL

MODEL QUESTION PAPER

S.No	Experiments	CO	PO
1	Write C program to calculate simple interest and compound interest.	D360.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
2	Write C program to find the solution of a quadratic equation.	D360.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
3	Write C program to find whether the given number is even or odd.	D360.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
4	Write C program to find the sum of series using 'While' loop.	D360.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
5	Write C program to perform the Arithmetic operation based on the numeric key press using switch case statement.(1-Addition,2- Subtraction,3–multiplication,4-Division).	D360.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
6	Write C program to find the biggest number among three numbers.	D360.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
7	Write C program to print Fibonacci series.	D360.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
8	Write C program to find factorial of given N numbers using function.	D360.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
9	Write C program to prepare the total marks for N students by reading the Name, Reg.No, Marks 1toMarks6 using array of structure.	D360.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
10	Write C program to swap the values of two variables.	D360.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
11	Write C program to calculate the sum and average of given three numbers using function.	D360.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
12	Write C program to sort the names in alphabetical order.	D360.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
13	Write C program to count the number of digits in a given integer and print the reverse number.	D360.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
14	Write C program for matrix addition.	D360.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
15	Write C program to print multiplication table.	D360.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
16	Write C program to print the college name 10 times.	D360.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
17	**Mini Project**	**D360.5**	**PO1,PO2,PO3,PO4 PO5,PO6,PO7**

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ECD370 SIMULATION PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

No.of weeks/ Semester: 16 weeks

Course	Instruction		Examination			
	Hours /week	Hours /semester	Marks			Duration
			Internal Assessment	Autonomous Examination	Total	
Simulation Practical	**4**	**64**	**25**	**100***	**100**	**3 Hours**

*** Examination will be conducted for 100 marks and it will be reduced to 75 marks.**

DETAILED ALLOCATION OF MARKS

Sl.No	DESCRIPTION	MARKS
1.	CIRCUIT DIAGRAM (MANUAL DIAGRAM)	25
2.	DEVELOPEMENT OF CIRCUIT DIAGRAM	25
3.	SIMULATION PERFORMANCE & PRINT OUT	35
4.	VIVA–VOCE	5
5.	MINI PROJECT	10
	TOTAL	**100**

Mini Project Evaluation (10 marks)

Breakup Details

1	Project Description	05
2	Project Demo	05
	Total	**10**

COURSE DESCRIPTION:

Every Electronic Engineer should have sound knowledge about the components used in Electronic Industry. This is vita lin R&D Department for chip level troubleshooting. To meet the industrial needs, diploma holders must be taught about the most fundamental subject, Electronic devices and Circuits Practical. By doing practical experience in this, they will be skilled in handling all types of electronic circuits and able to apply the skill in electronic systems. While designing electronic circuits to test a particular application we have to experiment it in a trial and error manner. In this situation, simulating the circuit is very useful to find out the results and select the suitable circuit elements.

LIST OF EQUIPMENTS: (FOR A BATCH OF 30 STUDENTS)

S.No.	Name of the Equipments	Required Nos.
1.	Simulation Tools Multisim/ PSpice/LabVIEW/TINA	-
2.	Desktop Computers	30 Nos.

OBJECTIVES:

- To study the Simulation Software (Multisim /PSpice/LabVIEW/TINA) and using the simulation of the given Circuits to design and verify the various electronic circuits and can further design the PCBs in the Computer.
- Develop the Mini Projects.

COURSE OUTCOMES

Course	**ECD370 SIMULATION PRACTICAL**
After successful completion of this course, the students should be able to	
D370.1	Design and verify the characteristics of Zener diode, rectifier circuits and Zener diode regulator circuits by using simulation tool.
D370.2	Design and verify the characteristics of CB transistor, CE transistor and emitter follower by using simulation tool.
D370.3	Design and verify the characteristics of RC coupled amplifier, Clippers and Clampers by using simulation tool.
D370.4	Design and verify the characteristics of RC phase shift oscillators, Hartley oscillator and Astable Multivibrator by using simulation tool.
D370.5	Design and verify the characteristics of gate triggering of SCR, UJT by using simulation tool and develop mini project with report.

ECD 370 SIMULATION PRACTICAL

Note: All experiments should be designed and verified through simulation tools like Multisim / PSpice/LabVIEW/TINA

1. Zener diode (Forward and Reverse bias characteristics)
2. Rectifier circuits (Half wave and Full wave Bridge Rectifiers with Capacitor filter)
3. Power supply with Zener diode as Regulator
4. Common Base transistor output characteristics
5. Common emitter amplifier (Implementation of Current Series negative feedback)
6. Emitter follower (Implementation of Voltage Series negative feedback)
7. RC Coupled amplifier (Implementation of the concept of multistage amplifier)
8. Clippers and Clampers
9. RC Phase shift oscillator (Medium frequency Sine wave generators)
10. Hartley oscillator (High frequency Sine wave generator)
11. Astable Multivibrator (Square or Rectangular wave generator)
12. Gate triggering of SCR with various gate currents.
13. Negative resistance characteristics of UJT
14. Mini Project

    The mini project is activity based and it may be given to group of maximum of six students for hands on experience and to create scientific temper.

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:

a) Attendance (Award of marks same as theory courses)	:	05 Marks
b) Procedure/ observation and tabulation/ Other Practical related Work	:	05 Marks
c)Tests	:	10 Marks
d) Student Centered Learning (SCL) work sheet	:	05 Marks
Total		25 Marks

LEARNING WEBSITES

1. https://www.androiderode.com/n-scheme-ece-simulation-practical-lab-manual-2021
2. https://www.etti.unibw.de
3. https://cds.cern.ch/record/987562/files/p363.pdf
4. https://www.androiderode.com/n-scheme-ece-simulation-practical-lab-manual-2021/
5. http://he-coep.vlabs.ac.in/List%20of%20experiments.html

CO- POs & PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
D370.1	3	3	3	3	3	3	3	3	3	3
D370.2	3	3	3	3	3	3	3	3	3	3
D370.3	3	3	3	3	3	3	3	3	3	3
D370.4	3	3	3	3	3	3	3	3	3	3
D370.5	3	3	3	3	3	3	3	3	3	3
D370 Total	15	15	15	15	15	15	15	15	15	15
Correlation Level	3	3	3	3	3	3	3	3	3	3

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

ECD370 SIMULATION PRACTICAL

MODEL QUESTION PAPER

Note: All experiments should be designed and verified through simulation tools like Multisim/ PSpice/LabVIEW/TINA

S.No	Experiments	CO	PO
1	Zener diode (Forward and Reverse bias characteristics).	D370.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
2	Rectifier circuits (Half wave and Full wave Bridge Rectifiers with Capacitor filter).	D370.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
3	Power supply with Zener diode as Regulator.	D370.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
4	Common Base transistor output characteristics.	D370.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
5	Common emitter amplifier (Implementation of Current Series negative feedback).	D370.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
6	Emitter follower (Implementation of Voltage Series negative feedback).	D370.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
7	RC Coupled amplifier (Implementation of the concept of multistage amplifier).	D370.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
8	Clippers and Clampers.	D370.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
9	RC Phase shift oscillator (Medium frequency Sine wave generators).	D370.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
10	Hartley oscillator (High frequency Sine wave generator).	D370.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
11	Astable Multivibrator (Square or Rectangular wave generator).	D370.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
12	Gate triggering of SCR.	D370.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
13	Negative resistance characteristics of UJT.	D370.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
14	**Mini Project**	**D370.5**	**PO1,PO2,PO3,PO4, PO5,PO6,PO7**

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ECD310 ELECTRONIC DEVICES AND CIRCUITS

MODEL QUESTION PAPER

Time: 3 Hrs **Max.Marks:100**

PART-A (10 X 3 = 30 Marks)					
Note: Answer all the questions. All questions carry equal marks.					
S.No	**Questions**	**UNIT**	**Bloom's Level**	**CO**	**PO**
1	Differentiate between Zener breakdown and Avalanche breakdown.	I	An	D310.1	PO1,PO2,PO3
2	Draw the symbol of LED and Photodiode.	I	An	D310.1	PO1,PO2,PO3
3	Compare BJT and FET.	II	E	D310.2	PO1,PO2,PO3
4	Mention the various methods of transistor biasing.	II	R	D310.2	PO1,PO2,PO3
5	What are the various types of negative feedback connections?	III	R	D310.3	PO1,PO2,PO3
6	What are the effects of negative feedback?(any two)	III	U	D310.3	PO1,PO2,PO3
7	Draw the symbol of SCR and TRIAC.	IV	An	D310.4	PO1,PO2,PO3
8	Expand (i) DIAC (ii)TRIAC.	IV	R	D310.4	PO1,PO2,PO3
9	Draw the circuit diagram of biased clipper.	V	An	D310.5	PO1,PO2,PO3
10	State any two applications of Monostable Multivibrator.	V	R	D310.5	PO1,PO2,PO3

PART-B (5 X 14 = 70 Marks)						
Note: Answer all questions choosing A or B in each question. All questions carry equal marks						
S.No	**Questions**	**Marks**	**UNIT**	**Bloom's Level**	**CO**	**PO**
11	(A) (i) Explain the working of Zener diode in Reverse bias. Draw its VI Characteristics.	07	I	U,An	D310.1	PO1,PO2,PO3
	(ii) Explain the working of LED. Draw its VI characteristics.	07	I	U	D310.1	PO1,PO2,PO3
	(OR)					
	(B) (i) Explain the working of Photo diode and draw its VI characteristics.	07	I	U,An	D310.1	PO1,PO2,PO3

	(ii) Explain the working of Zener diode Voltage regulator.	07	1	U	D310.1	PO1,PO2,PO3
12	(A) (i) Explain the working of Transistor as Switch	07	II	U	D310.2	PO1,PO2,PO3
	(ii) Explain the working of FET and draw its drain characteristics.	07	II	U,An	D310.2	PO1,PO2,PO3
	(OR)					
	(B) (i) Explain the working of UJT relaxation oscillator. Draw its output waveform .	07	II	U, An	D310.2	PO1,PO2,PO3
	(ii) Explain the working of CE Transistor amplifier .	07	II	U	D310.2	PO1,PO2,PO3
13	(A).(i) What are the effects of negative feedback?	07	III	R	D310.3	PO1,PO2,PO3
	(ii) Draw the circuit diagram in which current series feedback is introduced and Indicate in which place negative feedback is introduced.	07	III	An	D310.3	PO1,PO2,PO3
	(OR)					
	(B) (i) Explain the working of RC Phase shift oscillator.	07	III	U	D310.3	PO1,PO2,PO3
	(ii) Draw the circuit diagram and frequency response curve of RC coupled amplifier.	07	III	An	D310.3	PO1,PO2,PO3
14	(A) (i) Explain the gate triggering of SCR. Draw its VI characteristics	07	IV	U, An	D310.4	PO1,PO2,PO3
	(ii) Explain the working and draw the Bidirectional characteristics of DIAC.	07	IV	U,An	D310.4	PO1,PO2,PO3
	(OR)					
	(B) (i) Explain the working of TRIAC. Draw its VI characteristics.	07	IV	U,An	D310.4	PO1,PO2,PO3
	(ii) Explain the construction, working and characteristics of n channel MOSFET.	07	IV	U	D310.4	PO1,PO2,PO3
15	(A) (i) Explain the working of Schmitt trigger. Draw its input and output.	07	V	U,An	D310.5	PO1,PO2,PO3
	(ii) Explain the working of Astable Multivibrator.	07	V	U	D310.5	PO1,PO2,PO3
	(OR)					

	(B) (i) Explain the working of Biased Clipper and draw its output waveforms.	07	V	U,An	D310.5	PO1,PO2,PO3
	(ii) Explain the working of Voltage doubler and draw its output waveform.	07	V	U,An	D310.5	PO1,PO2,PO3

QUESTION PAPER SETTING

The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD320 ELECTRICAL CIRCUITS AND INSTRUMENTATION

MODEL QUESTION PAPER

TIME: 3 Hrs **Marks: 100**

PART-A (10 X 3 = 30 Marks)					
Note: Answer all the questions. All questions carry equal marks.					
S.No	**Questions**	**UNIT**	**Bloom's Level**	**CO**	**PO**
1	Define current. What is the unit of conductance?	I	R,U	D320.1	PO1, PO2, PO3
2	State maximum power transfer theorem.	I	R	D320.1	PO1, PO2, PO3
3	What is Resonance? Write the condition for resonance.	II	R, Ap	D320.2	PO1, PO2, PO3
4	Define resonant frequency. Write the formula for resonant frequency of series RLC circuit.	II	R, Ap	D320.2	PO1, PO2, PO3
5	Compare single phase and three phase power supply.	III	An	D320.3	PO1, PO2, PO3
6	What are the applications of transformer?	III	Ap	D320.3	PO1, PO2, PO3
7	Classify transducers.	IV	U	D320.4	PO1, PO2, PO3
8	What are the advantages of strain gauge?	IV	R	D320.4	PO1, PO2, PO3
9	Write short notes on Errors in measurement.	V	Ap	D320.5	PO1, PO2, PO3
10	Discuss about voltage sensitivity.	V	U	D320.5	PO1, PO2, PO3

	PART-B (5 X 14 = 70 Marks)					
	Note: Answer all questions choosing A or B in each question. All questions carry equal marks					
S. No	**Questions**	**Marks**	**UNIT**	**Bloom's Level**	**CO**	**PO**
11	A. (i).State Thevenin's theorem and explain.	07	I	R,U	D320.1	PO1, PO2, PO3
	(ii).State Maximum power transfer theorem and explain.	07	I	R,U	D320.1	PO1, PO2, PO3
	(OR)					
	B. (i).Explain superposition theorem with example.	07	I	U	D320.1	PO1, PO2, PO3
	(ii).Explain voltage division in series	07	1	U	D320.1	PO1, PO2,

	circuit and current division in parallel circuits.					PO3
12	A. (i) Derive an expression for the impedance in RLC series circuit.	07	II	Ap	D320.2	PO1, PO2, PO3
	(ii). Analyze RLC parallel circuit.	07	II	An	D320.2	PO1, PO2, PO3
	(OR)					
	B. (i). A 50 ohm resistor, 20 mH and a 50 μFcapacitor are all connected in parallel across a 50 V, 100 Hz supply. Calculate the total current drawn from the supply, the current for each branch and the total impedance of the circuit.	07	II	Ap	D320.2	PO1, PO2, PO3
	(ii) Derive the resonance frequency of series resonant circuit.	07	II	Ap	D320.2	PO1, PO2, PO3
13	A. (i).Explain the working principle of DC generator.	07	III	U	D320.3	PO1, PO2, PO3
	(ii).Explain the working principle of single phase induction motor.	07	III	U	D320.3	PO1, PO2, PO3
	(OR)					
	B.(i). Explain the working principle of stepper motor.	07	III	U	D320.3	PO1, PO2, PO3
	(ii).Explain the working principle of Universal motor.	07	III	U	D320.3	PO1, PO2, PO3
14	A. (i) Explain LVDT.	07	IV	U	D320.4	PO1, PO2, PO3
	(ii) Explain load cell.	07	IV	U	D320.4	PO1, PO2, PO3
	(OR)					
	B.(i).Draw the block diagram of CRO and explain.	07	IV	U	D320.4	PO1, PO2, PO3
	(ii).Explain the working principle of function generator.	07	IV	U	D320.4	PO1, PO2, PO3
15	A. (i).Explain the operation of PMMC instrument.	07	V	U	D320.5	PO1, PO2, PO3
	(ii).Explain the operation of Moving iron instrument.	07	V	U	D320.5	PO1, PO2, PO3
	(OR)					
	B. (i).Explain about thermo couple.	07	V	U	D320.5	PO1, PO2, PO3
	(ii).Explain about thermistor.	07	V	U	D320.5	PO1, PO2, PO3

QUESTION PAPER SETTING

The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as Presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD330 PROGRAMMING IN 'C'

MODEL QUESTION PAPER

TIME: 3 Hrs **MARKS: 100**

PART-A(10 X 3 = 30 Marks)					
Note: Answer all the questions. All questions carry equal marks					
S.No	**Questions**	**UNIT**	**Bloom's Level**	**CO**	**PO**
1	Differentiate low level language and high level language.	I	U	D330.1	PO1, PO2
2	Write the syntax for declaring variable and assigning value to variables.	I	R	D330.1	PO1, PO2
3	What are the operators in C?	II	R	D330.2	PO1,PO2
4	Discuss about precedence in expression.	II	U	D330.2	PO1,PO2
5	How do you declare one dimensional and two dimensional arrays?	III	U	D330.3	PO1,PO2
6	Discuss about strcmp (), strcpy ().	III	U	D330.3	PO1,PO2
7	Write short notes on arrays of structure.	IV	R	D330.4	PO1,PO2
8	Differentiate structure and union.	IV	U	D330.4	PO1,PO2
9	Write about call by value.	V	R	D330.5	PO1,PO2
10	Write the syntax for opening and closing a file.	V	R	D330.5	PO1,PO2

PART-C (5 X 14 = 70 Marks)						
Note: Answer all questions choosing A or B in each question. All questions carry equal marks						
S. No	**Questions**	**Marks**	**UNIT**	**Bloom's Level**	**CO**	**PO**
11	A. (i). Explain in detail about the structure of a C program with an example.	07	I	U	D330.1	PO1,PO2
	(ii). Explain in detail about flow chart.	07	I	U	D330.1	PO1,PO2
	(OR)					
	B. (i). Discuss about formatted and unformatted I/O statements in C.	07	I	U	D330.1	PO1,PO2

	(ii). Explain any 5 keywords in C with example.	07	1	R	D330.1	PO1,PO2,PO3
12	A. (i). Explain about break and continue statement.	07	II	U	D330.2	PO1,PO2 ,PO3
	(ii). Write a C program to find sum of series using while loop.	07	II	R	D330.2	PO1,PO2,PO3,PO4
	(OR)					
	B. (i). Write a C program to perform the arithmetic operation using switch case statement.	07	II	R	D330.2	PO1,PO2,PO3
	(ii).Explain conditional and bitwise operators.	07	II	U	D330.2	PO1,PO2,PO3
13	A. (i). Explain 1D and 2D array processing with examples.	07	III	U	D330.3	PO1,PO2,PO3
	(ii). Write a program sum of elements of array.	07	III	U	D330.3	PO1,PO2,PO3
	(OR)					
	B. (i).Explain about string handling functions.	07	III	U	D330.3	PO1,PO2,PO3
	(ii). Write the program for Matrix addition.	07	III	U	D330.3	PO1,PO2,PO3,PO4
14	A. (i) Explain about array of structure with example.	07	IV	U	D330.4	PO1,PO2,PO3
	(ii) Explain about declaring and initializing union.	07	IV	U	D330.4	PO1,PO2,PO3
	(OR)					
	B. (i). Explain structure within structure with example.	07	IV	U	D330.4	PO1,PO2,PO3
	(ii). Discuss about Union.	07	IV	U	D330.4	PO1,PO2,PO3
15	A. (i). Write a C program to find factorial of given N numbers using function.	07	V	U	D330.5	PO1,PO2,PO3,PO4
	(ii). Explain about types of in built functions.	07	V	U	D330.5	PO1,PO2,PO3

	(OR)					
	B. (i). Write a C program to count the number of digits in a number using function.	07	V	U	D330.5	PO1,PO2,PO3,PO4
	(ii). Write about Input/output operations on files and Error handling during I/O operations.	07	V	U	D330.5	PO1,PO2,PO3

QUESTION PAPER SETTING

The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as Presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD410 INDUSTRIAL ELECTRONICS

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 16 weeks

Course	Instruction		Examination			
			Marks			
Industrial Electronics	**Hrs/ Week**	**Hrs/ Semester**	**Internal Assessment**	**Autonomous Examination**	**Total**	**Duration**
	5	80	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

TOPICS AND ALLOCATION OF HOURS:

UNIT	TOPICS	NO. OF HOURS
I	Power devices and Trigger circuits	14
II	Converters and choppers	14
III	Inverters and applications	14
IV	Programmable logic controller	14
V	Building blocks of a robot	15
	Tests and Model Exam	9
TOTAL		**80**

COURSE DESCRIPTION:

The rationale behind this course is to give clear explanation of power devices and circuits that are widely used today in modern industry. It also gives exposure to PLCs & ROBOT's which can perform various control functions in industrial environments.

OBJECTIVES:

On completion of the following units of the syllabus contents, the students must be able to

- Study working principle of MOSFET,IGBT.
- Study the methods of triggering.
- Learn about converters and its types.
- Understand commutation concepts in SCR.
- Learn about choppers.
- Study about inverters and types.

- Understand the concept of HVDC.
- Know about SMPS.
- Understand about UPS and its types.
- Learn about PLC.
- Discuss about ladder diagrams.
- To understand the basic concepts associated with the design, functioning, applications and social aspects of robots.
- To study about the electrical drive systems and sensors used in robotics for various applications.

COURSE OUTCOMES

Course	**ECD410 INDUSTRIAL ELECTRONICS**
After successful completion of this course, the students should be able to	
D410.1	Understand the principle of working, VI characteristics and applications of power electronic devices - IGBT, MOSFET and GTO and learn triggering circuits.
D410.2	Learn the operation of converters and choppers, Buck –Boost Converter.
D410.3	Understand about the inverters and its applications.
D410.4	Analyze the basic concepts of Programmable Logic Controller and PLC functions.
D410.5	Understand the building blocks of a ROBOT and ROBOT sensor.

ECD410 INDUSTRIAL ELECTRONICS

UNIT- I

POWER DEVICES AND TRIGGER CIRCUITS **[14Hrs]**

1.1 POWER DEVICES

Insulated gate bipolar transistor(IGBT), [2 Hrs]

MOSFET and GTO [1 Hr]

Symbol, principle of working, VI characteristics and applications. [2 Hrs]

Comparison - between power MOSFET, power transistor and power IGBT [1 Hr]

1.2 TRIGGER CIRCUITS

Triggering of SCR - Gate triggering –Types –Concepts of DC triggering, [2 Hrs]

AC triggering, Pulse gate triggering – Pulse transformer in trigger circuit [1 Hr]

Electrical isolation by opto isolator [1 Hr]

Resistance ,capacitor firing circuit and waveform, [2 Hrs]

Synchronized UJT triggering (ramp triggering)circuit and waveform. [2 Hrs]

UNIT -II

CONVERTERS AND CHOPPERS (Qualitative treatment only) **[14Hrs]**

2.1 CONVERTERS

Converters – Definition – Single phase Half controlled bridge converter [2 Hrs]

with R load and RL load

Importance of flywheel diode –Single phase fully controlled bridge converter [2Hrs]

With Resistive load – voltage and current waveforms

Single phase fully controlled bridge converter with RL load – [2Hrs]

Voltage and current waveforms Commutation- [1 Hr]

Natural commutation – Forced commutation – Types

Buck –Boost Converters [1 Hr]

2.2 CHOPPERS

Chopper – Definition –principle of DC chopper operation [2 Hrs]

Typical chopper Circuit (Jones chopper) –Applications of DC chopper [2 Hrs]

Principle of working of single phase AC chopper -Chopper using MOSFET. [2 Hrs]

UNIT -III

INVERTERS & APPLICATIONS **[14Hrs]**

3.1 INVERTERS

Inverter with resistive load [2Hrs]

Single phase inverter with RL load –Methods to obtain sine wave output from an inverter-output voltage control in inverters [2Hrs]

McMurray inverter [2Hrs]

Advantages-Parallel [2Hrs]

3.2 INVERTERS APPLICATIONS

SMPS Types - Block diagram of SMPS – advantages and disadvantages. [2Hrs]

UPS-Type (ON Line, OFF Line), [2Hrs]

Comparison - Battery banks [2Hrs]

UNIT -IV

PROGRAMMABLE LOGIC CONTROLLER **[14 Hrs]**

4.1 BASICS OF PLC

Evolution – Advantages over relay logic [2 Hrs]

Introduction to PLC – Relays- Block diagram of PLC [2 Hrs]

PLC Programming Languages - Arithmetic Functions – (add, sub, mul, div, sqr) - Comparison of functions [2 Hrs

Basics of Input and output module(digital input and output module) [1Hr]

4.2 PLC FUNCTIONS

Logic functions - AND logic, OR logic, NAND logic, EX-OR logic [2 Hrs]

Symbols used in ladder logic diagram. [1 Hr**]**

Ladder programming – Ladder diagram for simple Systems [2Hrs]

Star delta starter, Conveyer control and Lift control [1Hr**]**

PLC interface with GSM-Applications of PLC [1 Hr**]**

UNIT –V

INTRODUCTION TO ROBOT **[15Hrs]**

5.1 BUILDING BLOCKS OF A ROBOT

Types of electric motors - DC, Servo, Stepper [2 Hrs]

specification, drives for motors [2 Hrs]

Speed& direction control and circuitry, Selection criterion for actuators, [2 Hrs]

direct drives, non-traditional actuators. [2 Hrs]

5.2 ROBOT SENSOR

Sensors for localization, navigation, [1 Hr]

obstacle avoidance and path planning in known and unknown environments [2 Hrs]

optical, inertial, thermal, chemical, biosensor, other common sensors; [2 Hrs]

Case study on choice of sensors and actuators for maze solving robot [2 Hrs]

and self-driving cars

Tests & Model Exam [9 Hrs]

TEXT BOOKS:

S.NO	TITLE	AUTHOR	PUBLISHER WITH EDITION
1.	Power Electronics	M.H.Rashid	PHI Publication-3rd Edition-2005
2.	Industrial Electronics and control	Biswanath Paul	PHI publications-2nd Edition -2010
3	Programmable Logic Controllers	Frank D.Petruzela	PHI publications-4 th Edition -2010
4	Power Electronics	Dr.P.S.Bimbhra	Khanna Publishers-2nd Edition -1998

REFERENCE BOOKS:

S.NO	TITLE	AUTHOR	PUBLISHER WITH EDITION
1.	Industrial & Power Electronics	Harish C.Rai	Umesh Publication, 5th Edition 1994
2.	Introduction to Robotics ,Analysis, Systems ,application	Saeed B.Niku	Pearson Educations,2002
3.	Introduction to Autonomous Mobile Robots	Roland Siegwart,illah Reza Noubakhsh	MIT Press, 2011

LEARNING WEBSITES

1. https://www.pdfdrive.com/industrial-electronics-e20252132.html/
2. https://frank.pocnet.net/other/Philips/Kretzmann_IndustrialElectronicsHandbook_1964.pdf
3. https://www.robotplatform.com/knowledge/sensors/types_of_robot_sensors.html
4. https://www.polycase.com/techtalk/electronics-tips/what-is-a-programmable-logic-controller.html
5. https://www.pdfdrive.com/rf-engineering-for-wireless-networks-hardware-antennas-and-propagation-communications-engineering-e184426215.html

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	-	**25 Marks**

CO-POs &PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
D410.1	3	3	3	3	3	2	2	3	2	2
D410.2	3	3	3	3	3	2	2	3	2	2
D410.3	3	3	3	3	3	2	2	3	2	2
D410.4	3	3	3	3	3	2	2	3	2	2
D410.5	3	3	3	3	3	2	2	3	2	2
D410Total	15	15	15	15	15	10	10	15	10	10
Correlation Level	3	3	3	3	3	2	2	3	2	2

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

****

ECD420 COMMUNICATION ENGINEERING

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 16 weeks

Course	Instruction		Examination			
			Marks			
Communication Engineering	**Hrs/ Week**	**Hrs/ Semester**	**Internal Assessment**	**Autonomous Examination**	**Total**	**Duration**
	5	80	25	100*	100	3Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

TOPICS AND ALLOCATION:

UNIT	TOPICS	NO. OF HOURS
I	Networks, Filters, Antenna and Propagation	15
II	Amplitude Modulation	14
III	Frequency Modulation	15
IV	Pulse Modulation	13
V	Audio , Video Systems and Displays	14
	Tests& Model Exam	9
TOTAL		80

COURSE DESCRIPTION:

Today communication engineering has developed to a great extent that there is always the need for study of various communication concepts. This course fulfills the need for students to have a thorough knowledge of Filters, various types of Antennas, modulations, audio systems, video systems and displays.

OBJECTIVES:

On completion of the following units of the syllabus contents, the students must be able to

- Understand the concepts of networks.
- Understand the applications of Filters.
- Know the Electro Magnetic Frequency Spectrum.
- Know the relationship between Wavelength and Frequency.
- Understand the principles of working of antennas.
- Understand the theory of Propagation.
- Understand the concept of modulation.

- Study Amplitude Modulation Process.
- Learn about different types of AM Transmitters & receivers.
- Study the Frequency Modulation Process.
- Learn about different types of FM Transmitters & Receivers.
- Understand the concept of Pulse Modulation.
- Learn about different type of Pulse Analog modulation Techniques.
- Learn about different type of Pulse Digital modulation Techniques.
- Learn Different types of Microphones.
- Learn Different types of Loudspeaker.
- Understand the principles of Monochrome & colour TV fundamentals.
- Understand the concept of Colour transmission and reception in PAL colour TV Receiver.
- Understand the concept of various types of displays.

COURSE OUTCOMES

Course	**ECD420 COMMUNICATION ENGINEERING**
After successful completion of this course, the students should be able to	
D420.1	Grasp the basic concepts Networks, filters, EM frequency spectrum, antenna and different types of propagation.
D420.2	Understand the fundamentals of Modulation, Amplitude Modulation, spectrum, signal diagram, AM transmitter and AM receiver.
D420.3	Understand the fundamentals of Frequency Modulation, spectrum, FM Transmitter and FM Receiver.
D420.4	Understand the fundamentals of Pulse Analog Modulation Techniques and Pulse Digital Modulation Techniques.
D420.5	Learn the basic concepts of audio and video systems –Microphones, Loud speakers, Monochrome TV, Colour television and different types of Displays. .

ECD420 COMMUNICATION ENGINEERING

UNIT-I

NETWORKS, FILTERS, ANTENNA AND PROPAGATION **[15 Hrs]**

3.1 SYMMETRICAL AND ASYMMETRICAL NETWORKS

Definition – Comparison [1 Hr]

characteristic impedance and propagation constant [1 Hr]

3.2 FILTERS

Definition , Types [1 Hr]

circuit elements and cut-off frequencies of Constant K

LPF ,HPF and BPF(Qualitative analysis only) –applications [2 Hrs]

3.3: ELECTROMAGNETIC FREQUENCY SPECTRUM

Electromagnetic Frequency Spectrum [1 Hr]

Types of Electro Magnetic Radiation and their applications [1 Hr]

3.4: RELATIONSHIP BETWEEN WAVELENGTH AND FREQUENCY [1 Hr]

3.5: ANTENNA

Definition – types of antenna: Mono pole and dipole antenna, [1 Hr]

Directional and Omni directional antenna ,Dipole arrays, Yagi antenna- parabolic

antenna-Smart antennas [1 Hr]

Antenna parameters: directive gain, directivity, radiation pattern [1 Hr]

and polarization- applications.

3.6: PROPAGATION

Types of Propagation - Concept, Frequency Range, Advantages, [1 Hr]

Applications of Ground wave propagation- sky wave and space wave propagation

Factors affecting the field strength in Ground wave propagation [1 Hr]

Effects of Atmosphere in Space wave propagation [1 Hr]

Definition of the terms in Sky wave propagation: Critical Frequency, [1 Hr]

MUF(Maximum Usable Frequency) and Skip distance.

UNIT–II

AMPLITUDE MODULATION **[14 Hrs]**

2.1 : INTRODUCTION TO MODULATION

Definition - Need for modulation-types of modulation-Electromagnetic [1 Hr]

Frequency Spectrum – Relationship between Wavelength and frequency [2 Hrs]

2.2 : AMPLITUDE MODULATION (AM)

Definition - Waveform representation of AM [1 Hr]

Expression for AM and modulation index [1 Hr]

Frequency spectrum of AM [1 Hr]

AM sidebands: DSB, SSB and VSB. [1 Hr]

2.3 AM TRANSMITTER

Types of transmitters [1 Hr]

high level AM transmitter and low level AM transmitter [2 Hrs]

SSB transmitter. [1 Hr]

2.4 AM RECEIVER

Super heterodyne receiver [2 Hrs]

Importance of IF in AM Receiver. Selection of IF (Intermediate Frequency) [1 Hr]

UNIT- III

3.1 FREQUENCY MODULATION [15 Hrs]

Definition-Waveform representation of Frequency modulation, [2 Hrs]

Expression for Frequency modulation and modulation index [2 Hrs]

Frequency spectrum of FM [1Hr]

Effects of modulation index in frequency spectrum. [1 Hr]

3.2 FM TRANSMITTERS :

Types of transmitters : Direct FM transmitter, [2 Hrs]

Indirect FM transmitter and stereophonic FM transmitter. [3 Hrs]

3.3 FM RECEIVER:

Stereophonic FM receiver-AFC [2 Hrs]

Comparison of FM and AM. [2 Hrs]

UNIT -IV

PULSE MODULATION [13 Hrs]

4.1 : INTRODUCTION

Definition- Types of Pulse modulation- [1 Hr]

Sampling and Quantization- [1 Hr]

Sampling theorem [1 Hr]

Nyquist sampling rate [1 Hr]

4.2 : PULSE ANALOG MODULATION TECHNIQUES

Generation and detection of PAM, [3 Hrs]

PWM,PPM [2 Hrs]

4.3 : PULSE DIGITAL MODULATION TECHNIQUES

PCM&DPCM- [2 Hrs]

Delta modulation-Adaptive Delta modulation [2 Hrs]

UNIT -V

AUDIO AND VIDEO SYSTEMS [14 Hrs]

1.1 MICROPHONES

Definition-Construction and performance of the following microphones: carbon - [2 Hrs]

moving coil and velocity ribbon. [1 Hr]

1.2 LOUD SPEAKERS

Construction and working of dynamic cone type [2Hrs]

Surround-sound systems. [1 Hr]

1.3 MONOCHROME TELEVISION

Scanning principles synchronization [1 Hr]

aspect ratio- composite video signal [1 Hr]

TV broadcasting standards [1 Hr]

1.4 COLOUR TV

Principles of colour transmission and reception- [1 Hr]

Block diagram and working of PAL [1 Hr]

Colour TV Receiver [1 Hr]

1.5: Displays

Construction and working principle of LED, [1 Hr]

OLED and Plasma display [1 Hr]

Tests & Model Exam [9 Hrs]

TEXT BOOKS:

S.NO	TITLE	AUTHOR	PUBLISHER WITH EDITION
1.	Transmission Lines & Networks	Umesh Sinha	Sathya Prakashan Publications – 5th edition 1992
2.	Radio Engineering - I	G.K.Mithal	Khana Publisher – 7thedition 1992

REFERENCE BOOKS:

Sl.No	Title	Author	Publisher with Edition
1.	Networks lines and fields	John D.Ryder	PHI ,II Edition 2005
2.	Electronic communication Systems	George Kennedy	TMH, 10 th reprint 2011
3.	Electronic Communication	Dennis Roddy John colen	PHI, II Edition 2005
4.	Fundamentals of Acoustics	Kingsler & frey	Wiley Eastern Ltd. 2 nd edition 1967
5.	TV and Video engineering	Arvind M.Dhake	TMH, 15 th reprint 2005.
6.	Communication Electronics – Principles and application -	Louis E Frenzel	Third Edition, Tata McGrawhill publication 2002
7.	Audio and Video system– Principles, maintenance and Troubleshooting	R.Gupta	Second Edition McGrawHill Education (P) Ltd-2010

LEARNING WEBSITES

1.http://www.freebookcentre.net/electronics-ebooks-download/Communication-Systems-by-Dr-Cong-Ling.html
2. https://engineeringbookspdf.com/category/communication-engineering-books/page/2
3. https://www.pdfdrive.com/communication-systems-engineering-communication-systems-engineering-program-d42880442.html
4. https://www.gadgetronicx.com/best-websites-to-learn-build-electronics
5.. https://en.wikibooks.org/wiki/Communication_Systems/Pulse_Amplitude_Modulation

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	-	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
D420.1	3	3	3	3	3	2	2	3	2	2
D420.2	3	3	3	3	3	2	2	3	2	2
D420.3	3	3	3	3	3	2	2	3	2	2
D420.4	3	3	3	3	3	2	2	3	2	2
D420.5	3	3	3	3	3	2	2	3	2	2
D420Total	15	15	15	15	15	10	10	15	10	10
Correlation Level	3	3	3	3	3	2	2	3	2	2

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

****

ECD430 ANALOG AND DIGITAL ELECTRONICS

TEACHING AND SCHEME OF EXAMINATION:

No. of weeks per semester: 16 weeks

Course	Instruction		Examination			
			Marks			
	Hrs/ Week	Hrs / Semester	Internal Assessment	Autonomous Examination	Total	Duration
Analog and Digital Electronics	4	64	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

TOPICS AND ALLOCATION OF HOURS:

UNIT	TOPICS	NO. OF HOURS
I	Linear ICs and OP-amps	10
II	A/D, D/A, Special Function ICs and IC Voltage Regulators	12
III	Boolean Algebra and Arithmetic operations	10
IV	Combinational and Sequential Logic Circuits	11
V	Memories	12
	Test &Model Exam	9
TOTAL		**64**

COURSE DESCRIPTION:

The course Analog and Digital Electronics holds applications in all branches of engineering instrumentation and Industrial Automation. This will impart in depth knowledge of Number Systems, Logics of Combinational &Sequential circuits and memories.

OBJECTIVES:

On completion of the following units of the syllabus contents, the students must be able to

- Understand the basics of operational amplifier.
- Know the op-amp applications.
- Know the waveform generator and Active filter.
- Know the concept of D/A and A/D converters.
- Know the applications of Special function IC, IC 555Timer.
- Understand various Number Systems used in Digital Circuits.
- Understand basic Boolean postulates and laws.
- Understand the De-Morgan's theorem.

- Understand the concept of Karnaugh Map.
- Learn about Basic logic Gates.
- Study about Boolean techniques.
- Learn the different digital logic families.
- Learn arithmetic circuits-Adder/ Subtractor
- Understand the encoder/decoder & MUX /DEMUX.
- Understand the concept of parity Generator and checker.
- Understand various types of flip-flops.
- Understand various types of counters.
- Understand various modes of shift registers.
- Understand various types of memories.

COURSE OUTCOMES

Course	**ECD430 ANALOG AND DIGITAL ELECTRONICS**
After successful completion of this course, the students should be able to	
D430.1	Know the concepts of Operational Amplifier, applications of OP-AMP and OP-AM P specifications.
D430.2	Analyze different types of A/D Converter, D/A Converter, special function ICs and IC voltage Regulators.
D430.3	Develop competence in analysis of Boolean algebra , arithmetic operations and arithmetic Circuits.
D430.4	Analyze different types of combinational and sequential logic circuits like Parity Generator and checker, Encoder, Decoder, multiplexer, demultiplexer, Counters and Shift Registers.
D430.5	Understand the classification of RAM and ROM Memories.

ECD430 ANALOG AND DIGITAL ELECTRONICS

UNIT I

LINEAR ICS AND OP-AMPS **[10Hrs]**

1.1: OPERATIONAL AMPLIFIER

Ideal Op-Amp – Block diagram and Characteristics [2 Hrs]

Op-amp parameters CMRR – Slew rate – [1 Hr]

Concept of Virtual ground [1 Hr]

1.2: APPLICATIONS OF OP-AMP

Inverting amplifier –Summing amplifier – Non inverting amplifier [1 Hr]

Voltage follower - Comparator – Zero crossing detector [1 Hr]

Integrator – Differentiator- waveform generation (Schmitt Trigger only) [1 Hr]

RC Low pass Active filter. [1 Hr]

1.3: OP-AMP SPECIFICATIONS

OP-amp 741 – Symbol – Pin diagram – Specifications [2 Hrs]

UNIT -II

A/D, D/A ,SPECIAL FUNCTION ICs AND IC VOLTAGE REGULATORS **[12 Hrs]**

2.1 : SAMPLING AND QUANTIZATION [1 Hr]

2.2 : A/D CONVERTER

Analog to digital conversion using Ramp method [1 Hr]

Successive approximation method – Dual slope method [1 Hr]

Specifications of A/D converter [1 Hr]

2.3: D/A CONVERTER

Basic concepts – Weighted Resistor D/A converter [1 Hr]

R-2R Ladder D/A converter – Specifications of DAC IC [1 Hr]

2.4 :SPECIAL FUNCTION ICS

2.4.1 :IC 555 Timer – Pin diagram - Functional Block diagram of IC 555 in [1 Hr]

Astable and Monostable Multivibrator mode - Schmitt trigger using IC 555

2.4.2:IC 565-PLL-Pin diagram-Functional Block diagram of IC 565 [1 Hr]

2.4.3:IC 566-VCO-Pin diagram-Functional Block diagram of IC 566 [1 Hr]

2.5.: IC VOLTAGE REGULATORS

Positive IC Voltage Regulators: 78XX [1 Hr]

Negative IC Voltage Regulators: 79XX and General purpose [2 Hrs]

IC Voltage Regulators using LM 723.

UNIT- III

BOOLEAN ALGEBRA AND ARITHMETIC OPERATIONS [10Hrs]

3.1: NUMBER SYSTEMS

Decimal – Binary – Octal – Hexadecimal – BCD –

Conversion from one number system to other – [1 Hr]

Boolean Algebra – Basic laws and Demorgan's Theorems [1 Hr]

3.2: UNIVERSALGATES

Realization of basic logic gates using universal gates NAND and NOR –

Tristate Buffer circuit [2 Hrs]

3.3: PROBLEMS USING 2, 3, AND 4 VARIABLES

Boolean expression for outputs –

Simplification of Boolean expression using Karnaugh map (up to 4 variables)- [1 Hr]

Constructing logic circuits for the Boolean expressions [1 Hr]

3.4: ARITHMETIC OPERATIONS

Binary Addition-Binary Subtraction-

1's compliment and 2's compliment- [1 Hr]

Signed binary numbers [1 Hr]

3.5: ARITHMETIC CIRCUITS

Half Adder-Full Adder- [1 Hr]

Half Subtractor-Full Subtractor [1 Hr]

UNIT-IV

COMBINATIONAL AND SEQUENTIALLOGIC CIRCUITS [11 Hrs]

4.1 PARITY GENERATOR AND CHECKER [1 Hr]

4.2 DECIMAL TO BCD ENCODER [1 Hr]

4.3 3 to 8 DECODER [1 Hr]

4.4 MULTIPLEXER [1 Hr]

4 to 1 Multiplexer

4.5 DEMULTIPLEXER [1 Hr]

1 to 4 Demultiplexer

4.6: FLIP-FLOPS (FF) [2 Hrs]

RS FF– JK FF: Master Slave FF and Edge triggered FF – D and T FF

4.7 COUNTERS

4 bit Asynchronous Up Counter –Mod N counter – [1 Hr]

Decade counter –4 bit Synchronous Up counter [1 Hr]

4.8 SHIFT REGISTER

4 bit shift register – serial in serial out

4 bit Serial in parallel out

4 bit parallel in parallel out

4 bit parallel in serial out [2 Hrs]

UNIT -V

MEMORIES **[12 Hrs]**

5.1 CLASSIFICATION OF MEMORIES

5.2 RAM

RAM organization- [1 Hr]

Address Lines and Memory Size- [1 Hr]

Read/write operations-Static RAM- [1 Hr]

Bipolar RAM cell- Dynamic RAM- [1 Hr]

SD RAM- DDR RAM. [2 Hrs]

5.3 ROM

ROM organization-Expanding memory- [2 Hrs]

PROM- EPROM- and EEPROM- [2 Hrs]

Flash memory- Anti Fuse Technologies. [2 Hrs]

Tests & Model Exam **[9 Hrs]**

TEXT BOOKS:

S.No	Title	Author	Publisher with Edition
1.	Principles of Digital Electronics	K.Meena	PHI – 2011
2.	Modern Digital Electronics	R.P.Jains	TMH -2003

REFERENCE BOOKS:

S.No	Title	Author	Publisher with Edition
1.	Digital principles & Applications	Albert Paul Malvino& Donald P.Leach	TMH - 4th Edition 2002
2.	Digital Electronics	William H.Gothmann	Prentice Hall of India – 2nd Edition,1995
3.	Linear integrated circuits	B.Suseela&T.R.Ganeshbabu	Scitechpublications-2018
4.	Digital Electronics	Roger L.Tokheim Macmillan	McGraw hill -1994
5.	Integrated circuits	K.R.Botkar	Khanna publisher's-1996

LEARNING WEBSITES

1. https://www.geeksforgeeks.org/digital-electronics-logic-design-tutorials/

2.https://www.tutorialspoint.com/digital_electronics/index.asp

3. https://en.wikibooks.org/wiki/Digital_Electronics

4.https://www.electrical4u.com/digital-electronics/

5.https://www.factmonster.com/dk/encyclopedia/science/digital-electronics

CONTINUOUS INTERNAL ASSESSMENT:

Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	-	**25 Marks**

CO-POs &PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
D430.1	3	3	3	3	3	2	2	3	2	2
D430.2	3	3	3	3	3	2	2	3	2	2
D430.3	3	3	3	3	3	2	2	3	2	2
D430.4	3	3	3	3	3	2	2	3	2	2
D430.5	3	3	3	3	3	2	2	3	2	2
D430Total	15	15	15	15	15	10	10	15	10	10
Correlation Level	3	3	3	3	3	2	2	3	2	2

Correlation level 1- Slight (low)
Correlation level 2- Moderate (Medium)
Correlation level 3- Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

****

ECD440 E-VEHICLE TECHNOLOGY & POLICY

TEACHING AND SCHEME OF EXAMINATION

No of weeks per semester: 16 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/ Week	Hrs / Semester	Internal Assessment	Autonomous Examination	Total	
E Vehicle Technology &Policy	4	64	25	100*	100	3 Hrs

*** Examination will be conducted for 100 marks and it will be reduced to 75 marks for result.**

TOPICS AND ALLOCATION OF HOURS:

UNIT	TOPICS	NO. OF HOURS
I	Environmental impact and history & Electric vehicle Types	11
II	Electric vehicle & Drive System	11
III	Energy Storages, Charging System, Effects and Impacts	11
IV	Electric Mobility Policy Frame Work	11
V	Tamil Nadu E-Vehicle Policy 2019	11
	Test& Model Exam	9
TOTAL		**64**

COURSE DESCRIPTION:

The world is transitioning to cleaner mobility options with the aim at improving air quality and reducing dependency on fossil fuels. Electric Vehicles (EVs) have emerged a popular clean mobility choice to reduce emissions. EVs are powered fully or partially by batteries, they can help to reduce dependence on fossil fuels also air quality. Tamil Nadu is one of the most advanced states in India. Tamil Nadu has a highly developed industrial eco-system and is very strong in sectors like automobiles and auto-components. Many globally renowned companies have setup their manufacturing facilities in Tamil Nadu. Due to the rapid depletion of fossil fuel and increase in fuel cost, environmental pollution, the shift to clean transport is necessary. This subject introduced by keeping all the above factors.

OBJECTIVES:

- To learn the environmental impact and history of Electric Vehicles.
- To understand the concept of Electric Vehicle and its types.
- To study the configurations of Electric Vehicles.
- To acquire knowledge about Energy Storages, Charging System, Effects and Impacts.
- To appreciate the Electric Mobility Policy Frame work India and EV Policy Tamil Nadu 2019.

COURSE OUTCOMES

Course	**ECD440 E-VEHICLE TECHNOLOGY & POLICY**
After successful completion of this course, the students should be able to	
D440.1	Know the Environmental impact, history and different types of Electric vehicle.
D440.2	Understand the basics of electric vehicles and Electric Propulsion Systems.
D440.3	Analyze the different types of energy storages, chargers for electric vehicles and explain effects and impacts of electric vehicles.
D440.4	Understand the Electric mobility and Policy frame work for Electric Vehicles.
D440.5	Know the Tamil Nadu E-Vehicle Policy 2019.

ECD440 E-VEHICLE TECHNOLOGY & POLICY

UNIT I

ENVIRONMENTAL IMPACT AND HISTORY & ELECTRIC VEHICLE TYPES [11 Hrs]

1.1 ENVIRONMENTAL IMPACT AND HISTORY

Environmental impact of conventional vehicle - Air pollution – [1 Hr]

Petroleum resources – History of Electric vehicles & Hybrid Electric Vehicles – [1 Hr]

Conventional drive train system – Rear Wheel, Front Wheel and All wheel – [1 Hr]

Parts of Drive train system [1 Hr]

1.2 ELECTRIC VEHICLE TYPES

Introduction to Battery Electric Vehicle (BEV) – Definition BEV – [2 Hrs]

Necessity BEV – Different between BEV and Conventional Vehicle – [1 Hr]

Advantages of BEV - Block diagram of BEV- [2 Hrs]

Hybrid electric Vehicle (HEV) - Plug-in Hybrid Electric Vehicle (PHEV)- [1 Hr]

Fuel Cell Electric Vehicle (FCEV) – Description [1 Hr]

UNIT II

ELECTRIC VEHICLE & DRIVE SYSTEM [11 Hrs]

2.1 ELECTRIC VEHICLES

Configurations of Electric Vehicle – Performance of Electric Vehicles – [1 Hr]

Tractive Effort in Normal Driving-energy consumption [1 Hr]

Hybrid Electric Vehicles Concept of Hybrid electric drive trains [1 Hr]

Architecture of Hybrid Electric Drive trains – Series, Parallel and Series & Parallel [2 Hrs]

2.2 ELECTRIC PROPULSION SYSTEMS

Types of EV motors - DC motor drives– [2 Hrs]

Permanent Magnetic Brush Less DC Motor Drives (BLDC) – [1 Hr]

Principles, Construction and Working – Hub motor Drive system – [1Hr]

Merits and Demerits of DC motor drive, BLDC motor drive [2 Hrs]

UNIT III

ENERGY STORAGES, CHARGING SYSTEM, EFFECTS AND IMPACTS [11 Hrs]

3.1 ENERGY STORAGES

Electrochemical Batteries – Battery Technologies – [1 Hr]

Construction and working of Lead Acid Batteries, [1 Hr]

Nickel Based Batteries and Lithium Based Batteries [1 Hr]

Role of Battery Management System (BMS)– Battery pack development Technology– [1 Hr]

Cell Series and Parallel connection to develop battery pack. [1 Hr]

3.2 CHARGING

Battery Charging techniques –Constant current and Constant voltage,

Trickle charging – [1 Hr]

Battery Swapping Techniques – DC charging – [1 Hr]

Wireless charging – Maintenance of Battery pack – [1 Hr]

Latest development in battery chemistry [1 Hr]

3.3 EFFECTS AND IMPACTS

Effects of EV – Impacts on Power grid – [1 Hr]

Impacts on Environment – Impacts on Economy [1 Hr]

UNIT IV

ELECTRIC MOBILITY POLICY FRAME WORK [11 Hrs]

Government of India Electric Mobility Policy Frame work – [1 Hr]

Global Scenario of EV adoption – Electric mobility in India – [2 Hrs]

National Electric Mobility Mission Plan 2020 – [1 Hr]

Action led by Original Equipment Manufacturers – [1 Hr]

Need of EV Policy-Advantage of EV Eco system – [1 Hr]

Scope and Applicability of EV Policy – [1 Hr]

ARAI Standards for Electric Vehicle – AIS 038, AIS 039 &AIS 123- [2 Hrs]

Key Performance Indicator-Global impact – Trends and Future Developments [2 Hrs**]**

UNIT V

TAMIL NADU E-VEHICLE POLICY 2019 [11 Hrs]

Tamil Nadu E-vehicle Policy 2019 [2 Hrs]

Vehicle Population in Tamil Nadu – [1 Hr]

Objectives of EV Policy – Policy Measures – [2 Hrs]

Demand side incentives – [1 Hr]

Supply side incentives to promote EV manufacturing- [1 Hr]

Revision of Transport Regulation of EV – [1 Hr]

City building codes – Capacity Building and Skilling – [1 Hr]

Charging structure – implementing agencies- [1 Hr]

R&D and Business Incubation – Recycling Ecosystem – Battery and EVs [1 Hr]

Tests & Model Exam **[9 Hrs]**

TEXT BOOKS

S.No	Title	Author	Publisher with Edition
1.	Electric Vehicles - A future Projection	-	CII October 2020 report.
2.	Design and analysis of aluminum/air battery system for electric vehicles,	Shaohua Yang, Harold Knickle,	Elsevier
3.	Propelling Electric Vehicles in India, Technical study of Electric Vehicles and Charging Infrastructure	-	-
4.	Zero emission vehicles (ZEVs): towards a policy framework	-	Nti Aayog
5.	Faster adoption of electric vehicles in India: perspective of consumers and industry	-	The Energy and Resources Institute, New Delhi.
6.	India EV Story: Emerging Opportunities by Innovation Norway.	-	-
7.	Automotive Industry Standards – AIS 038, AIS 039 & AIS 123 – Manual	-	-

REFERENCE BOOKS

S.No	Title	Author	Publisher with Edition
1.	Modern Electric, Hybrid Electric and Fuel Cell Vehicles	Mehrdad Ehsani, Yimin Gao, Sebastien E.Gay, Ali Emadi,	CR Press, London, NewYork
2.	Comparison of Electric and Conventional Vehicles in Indian Market:Total Cost of Ownership, Consumer Preference and Best Segment for Electric Vehicle (IJSR)	AkshatBansal, Akriti Agarwal	-
3.	A Comprehensive Study of Key Electric Vehicle (EV) Components, Technologies, Challenges, Impacts, and Future Direction of Development (MDPI),	Fuad Un-Noor, Sanjeevikumar Padmanaban, Lucian Mihet-Popa, Mohammad Nurunnabi Mollah and EklasHossain.	-

LEARNING WEBSITES

1. https://engineeringbookspdf.com/category/electrical-engineering-books/electric-vehicle/
2. http://www.iqytechnicalcollege.com/BAE%20685-Electric%20Vehicle%20Technology.pdf
3. https://afdc.energy.gov/vehicles/electric_maintenance.html
4. https://www.pdfdrive.com/the-advent-of-unmanned-electric-vehicles-the-choices-between-e-mobility-and-immobility-e186679004.html

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

- Attendance - 5 Marks
- Test - 10 Marks
- Assignment - 5 Marks
- Seminar - 5 Marks

Total - 25 Marks

CO-POs &PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
D440.1	3	3	3	3	3	3	3	3	2	2
D440.2	3	3	3	3	3	3	3	3	2	2
D440.3	3	3	3	3	3	3	3	3	2	2
D440.4	3	3	3	3	3	3	3	3	2	2
D440.5	3	3	3	3	3	3	3	3	2	2
D440Total	15	15	15	15	15	15	15	15	10	10
Correlation Level	3	3	3	3	3	3	3	3	2	2

Correlation level 1- Slight (low)
Correlation level 2- Moderate (Medium)
Correlation level 3- Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD450 INDUSTRIAL ELECTRONICS PRACTICAL

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester: 16 Weeks

Course	Instruction		Examination			
			Marks			Duration
Industrial Electronics Practical	Hrs/ Week	Hrs/ Semester	Internal Assessment	Autonomous Examination	Total	
	5	80	25	100*	100	3Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

DETAILED ALLOCATION OF MARKS

SL.NO	DESCRIPTION	MARKS
1	CIRCUIT DIAGRAM	25
2	CONNECTION	25
3	EXECUTION & HANDLING OF EQUIPMENT	25
4	OUTPUT /RESULT	10
5	VIVA–VOCE	5
6	MINI PROJECT	10
	TOTAL	**100**

Mini Project Evaluation (10 marks)

Breakup Details

1	Project Description	05
2	Project Demo	05
	Total	**10**

COURSE DESCRIPTION

The rationale behind the modifying this course is to give clear explanation of power devices and circuits that are widely used today in modern industry. It also gives exposure to PLCs &Inverters which can perform various control functions in industrial environments.

EQUIPMENTS REQUIRED: (FOR A BATCH OF 30 STUDENTS)

S.No	Name of the Equipment	Range	Required Nos
1	Regulated Power supply	0-30V	5
2	Dual trace CRO	-	2
3	Signal generator	-	2
4	PAM kit	-	1
5	PCM kit	-	1
6	PLC's	-	5
7	Computers	-	5
8	Software For PLC	-	-
9	Multimeter		10

OBJECTIVES:

On completion of all the experiments, the students must be able to

- Construct Phase control characteristics of SCR and test a commutation circuit.
- Construct a Lamp dimmer using TRIAC .
- Construct and test a MOSFET based PWM chopper circuit
- Construct and test an IC based buck converter using PWM
- Write and implement a simple ladder logic program using digital inputs and outputs for PLC
- Write and implement a simple ladder logic program for interfacing a lift control with PLC.
- Write and implement a simple ladder logic program for interfacing a conveyer control with PLC
- Write and implement a simple ladder logic program using timer and counter with branching and subroutines with PLC.
- Construct and draw the VI characteristics of IGBT.
- Construct and draw the VI characteristics of Power MOSFET
- Construct and draw single phase half controlled bridge converter with resistive load
- Construct and design a fan regulator using TRIAC and DIAC
- Construct and test the Single phase AC voltage controller using simulation tool
- Develop the Mini Project.

COURSE OUTCOMES

Course	**ECD450 INDUSTRIAL ELECTRONICS PRACTICAL**
After successful completion of this course, the students should be able to	
D450.1	Construct and Test the Phase control characteristics and commutation circuit, Lamp dimmer using TRIAC, MOSFET based PWM Chopper and IC based buck converter using PWM.
D450.2	Write and implement PLC Ladder logic program using digital inputs and outputs, Lift control interfacing a conveyer control with PLC, Ladder programmes with counter and timer with branching and subroutines.
D450.3	Construct and draw the VI characteristics of IGBT and Power MOSFET
D450.4	Design Single phase half controlled bridge converter with resistive Load and a fan regulator using TRIAC and DIAC.
D450.5	Construct and test the Single phase AC Voltage controller using simulation tool and develop the mini project with report.

ECD450 INDUSTRIAL ELECTRONICS PRACTICAL

1. Phase control characteristics of SCR and testing a commutation circuit.
2. Construct a Lamp dimmer using TRIAC (in Bread Board Only)
3. Construct and test a MOSFET based PWM chopper circuit
4. Construct and test an IC based buck converter using PWM
5. Write and implement a simple ladder logic program using digital inputs and outputs for PLC
6. Write and implement a simple ladder logic program for interfacing a lift control with PLC.
7. Write and implement a simple ladder logic program for interfacing a conveyer control with PLC
8. Write and implement a simple ladder logic program using timer and counter with branching and subroutines with PLC.
9. Construct and draw the VI characteristics of IGBT.
10. Construct and draw the VI characteristics of Power MOSFET
11. Construct and draw single phase half controlled bridge converter with resistive load
12. Construct and design a fan regulator using TRIAC and DIAC
13. Construct and test the Single phase AC voltage controller using simulation tool
14. Mini Project

The mini project is activity based and it may be given to group of maximum of six students for hands on experience and to create scientific temper.

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:

a) Attendance (Award of marks same as theory courses)	:	05 Marks
b) Procedure/ observation and tabulation/ Other Practical related Work	:	05 Marks
c)Tests	:	10 Marks
d) Student Centered Learning (SCL) work sheet	:	05 Marks
Total		25 Marks

LEARNING WEBSITES

1. https://gpmayurbhanj.org.in/wp-content/uploads/2020/07/Power-Electronics-Lab-PLC-Lab-5th-sem.pdf
2. https://www.hit.ac.in/download/LAB/EE/PE_LAB_JKM.pdf
3. http://www.freebookcentre.net/electronics-ebooks-download/Communication-Systems-by-Dr-Cong-Ling.html
4. https://www.electronicshub.org/electronics-mini-project-circuits
5. http://plc-coep.vlabs.ac.in/List%20of%20experiments.html

CO- POs & PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
D450.1	3	3	3	3	3	3	3	3	2	3
D450.2	3	3	3	3	3	3	3	3	2	3
D450.3	3	3	3	3	3	3	3	3	2	3
D450.4	3	3	3	3	3	3	3	3	2	3
D450.5	3	3	3	3	3	3	3	3	2	3
D450.5Total	15	15	15	15	15	15	15	15	10	15
Correlation Level	3	3	3	3	3	3	3	3	2	3

Correlation level 1- Slight (low)
Correlation level 2- Moderate (Medium)
Correlation level 3- Substantial (high)

ECD450 INDUSTRIAL ELECTRONICS PRACTICAL

MODEL QUESTION PAPER

S.No	Experiments	CO	PO
1	Phase control characteristics of SCR and testing a commutation circuit.	D450.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
2	Construct a Lamp dimmer using TRIAC (in Bread Board Only).	D450.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
3	Construct and test a MOSFET based PWM chopper circuit.	D450.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
4	Construct and test an IC based buck converter using PWM.	D450.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
5	Write and implement a simple ladder logic program using digital inputs and outputs for PLC.	D450.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
6	Write and implement a simple ladder logic program for interfacing a lift control with PLC.	D450.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
7	Write and implement a simple ladder logic program for interfacing a conveyer control with PLC.	D450.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
8	Write and implement a simple ladder logic program using timer and counter with branching and subroutines with PLC.	D450.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
9	Construct and draw the VI characteristics of IGBT.	D450.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
10	Construct and draw the VI characteristics of Power MOSFET.	D450.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
11	Construct and draw single phase half controlled bridge converter with resistive load.	D450.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
12	Construct and design a fan regulator using TRIAC and DIAC.	D450.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
13	Construct and test the Single phase AC voltage controller using simulation tool	D450.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
14	**Mini Project**	**D450.5**	**PO1,PO2,PO3,PO4, PO5,PO6,PO7**

ECD460 COMMUNICATION ENGINEERING PRACTICAL

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester: 16 Weeks

Course	Instruction		Examination			
Communication Engineering Practical	Hrs. Week	Hrs Semester	Marks			Duration
	4	64	Internal Assessment	Autonomous Examination	Total	
			25	100*	100	3Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

DETAILED ALLOCATION OF MARKS

S.No	DESCRIPTION	MARKS
1	CIRCUIT DIAGRAM	25
2	CONNECTION	25
3	EXECUTION & HANDLING OF EQUIPMENT	25
4	OUTPUT /RESULT	10
5	VIVA–VOCE	5
6	MINI PROJECT	10
TOTAL		**100**

Mini Project Evaluation (10 marks)

Breakup Details

1	Project Description	05
2	Project Demo	05
	Total	**10**

COURSE DESCRIPTION:

Every Electronics Engineer should have sound knowledge about the components used in Electronics Industry. This is vital in R&D Department for chip level troubleshooting. To meet the telecommunication industrial needs, diploma holders must be taught about the fundamental subject, Communication Engineering Practical. By doing practical experience in this, they will be skilled in handling all types of Communication circuits and able to apply the skill in trouble shooting of Audio and Video Systems and all electronic systems in various applications.

EQUIPMENTS REQUIRED: (FOR A BATCH OF 30 STUDENTS)

S. No	Name of the Equipments	Range	Required Nos
1.	Regulated power supply	0-30V	10
2.	Signal generators	-	10
3.	Dual trace CRO	60 MHZ	5
4.	Decade Resistance Box	0 – 100 K Ohm	5
5.	Decade Capacitance Box	0 – 100uF	5
6.	Decade Inductance Box	0 – 10H	5
7.	Desk Top Computer	-	2
8.	Dynamic cone Loudspeaker	-	2
9.	Moving coil Microphone	-	1
10.	Velocity Ribbon Microphone	-	1
11.	Software Tool	Multisim/OrCAD/Lab View	

OBJECTIVES:

On completion of the following experiments, the students must be able to

- Construct and test the performance of symmetrical T and π attenuators .
- Construct and test the performance of passive Low pass and High pass filters. Find out the cut-off frequency from the frequency response characteristics.
- Construct and test the performance of Band pass filter. Find out the cut-off frequencies and find the Bandwidth from the frequency response characteristics.
- Construct and test the performance of series and shunt equalizers.
- Construct and test the performance of Amplitude Modulator.
- Construct and test the performance of AM linear diode detector.
- Construct and test the performance of Pulse Width Modulator(PWM).
- Construct and test the performance of Pulse Position Modulator(PPM).
- Determine the directional characteristics of Moving Coil Microphone.
- Determine the directional characteristics of Dynamic cone Loudspeaker.
- Determine the frequency response characteristics of Two way cross over network.
- Design the PCB of AM modulator using simulation tools like Multsim/OrCAD/Labview.
- Determine the frequency response characteristics of Three way cross over network .
- Develop the Mini Project.

COURSE OUTCOMES

Course	**ECD460Communication Engineering Practical**
After successful completion of this course, the students should be able to	
D460.1	Construct and test the performance of symmetrical T and Pi attenuators, frequency response characteristics of Passive Low pass ,high pass filters and band pass filters.
D460.2	Construct and test the performance of series and shunt equalizers .
D460.3	Construct and test the performance of Amplitude modulator ,AM Linear diode detector ,Pulse Width Modulator(PWM) and Pulse Position Modulator(PPM) .
D460.4	Determine the directional characteristics of Moving coil Microphone, Dynamic cone Loud speaker and frequency response characteristics of Two way cross over network.
D460.5	Design the PCB of AM modulator and determine the frequency response characteristics of the three way cross over network using simulation tools and develop the mini project with report.

ECD460 COMMUNICATION ENGINEERING PRACTICAL

Note: At least 9 experiments should be constructed using breadboard/soldering

1. Construct and test the performance of symmetrical T and π attenuators .
2. Construct and test the performance of passive Low pass and High pass filters. Find out the cut-off frequency from the frequency response characteristics.
3. Construct and test the performance of Band pass filter. Find out the cut-off frequencies and find the Bandwidth from the frequency response characteristics.
4. Construct and test the performance of series and shunt equalizers.
5. Construct and test the performance of Amplitude Modulator.
6. Construct and test the performance of AM linear diode detector.
7. Construct and test the performance of Pulse Width Modulator(PWM).
8. Construct and test the performance of Pulse Position Modulator(PPM).
9. Determine the directional characteristics of Moving Coil Microphone.
10. Determine the directional characteristics of Dynamic cone Loudspeaker.
11. Determine the frequency response characteristics of Two way cross over network.
12. Design the PCB of AM modulator using simulation tools like Multsim/OrCAD/Labview.
13. Determine the frequency response characteristics of Three way cross over network .
14. Mini Project

The mini project is activity based and it may be given to group of maximum of six students for hands on experience and to create scientific temper

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:

a) Attendance (Award of marks same as theory courses)	:	05 Marks
b) Procedure/ observation and tabulation/ Other Practical related Work	:	05 Marks
c)Tests	:	10 Marks
d) Student Centered Learning (SCL) work sheet	:	05 Marks

Total		25 Marks

LEARNING WEBSITES

1. https://www.academia.edu/40527607/EEC_112_Communication_Electronics_Laboratory_Manual
2.https://mrcet.com/downloads/ECE/labmanuals/DIGITAL%20COMMUNICATIONS%20LAB.pdf
3.http://veltechengg.com/wp-content/uploads/2019/08/COMM-SYS-LAB-MANUAL.pdf
4.http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.718.5382&rep=rep1&type=pdf

CO- POs & PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
D460.1	3	3	3	3	3	3	3	3	3	3
D460.2	3	3	3	3	3	3	3	3	3	3
D460.3	3	3	3	3	3	3	3	3	3	3
D460.4	3	3	3	3	3	3	3	3	3	3
D460.5	3	3	3	3	3	3	3	3	3	3
D460 Total	15	15	15	15	15	15	15	15	15	15
Correlation Level	3	3	3	3	3	3	3	3	3	3

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

ECD460 COMMUNICATION ENGINEERING PRACTICAL

MODEL QUESTION PAPER

S.No	Experiments	CO	PO
1	Construct and test the performance of symmetrical T and π attenuators.	D460.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
2	Construct and test the performance of passive Low pass and High pass filters. Find out the cut-off frequency from the frequency response characteristics.	D460.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
3	Construct and test the performance of Band pass filter. Find out the cut-off frequencies and find the Bandwidth from the frequency response characteristics.	D460.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
4	Construct and test the performance of series and shunt equalizers.	D460.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
5	Construct and test the performance of Amplitude Demodulator.	D460.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
6	Construct and test the performance of AM linear diode detector.	D460.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
7	Construct and test the performance of Pulse Width Modulator(PWM).	D460.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
8	Construct and test the performance of Pulse Position Modulator(PPM).	D460.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
9	Determine the directional characteristics of Moving Coil Microphone.	D460.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
10	Determine the directional characteristics of Dynamic cone Loudspeaker.	D460.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
11	Determine the frequency response characteristics of Two way cross over network.	D460.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
12	Design the PCB of AM modulator using simulation tools like Multisim/ OrCAD/Labview.	D460.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
13	Determine the frequency response characteristics of Three way cross over network .	D460.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
14	**Mini Project**	**D460.5**	**PO1,PO2,PO3,PO4, PO5,PO6,PO7**

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ECD470 ANALOG AND DIGITAL ELECTRONICS PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

No. of weeks per semester: 16 weeks

Course	Instruction		Examination			
	Hrs/Week	Hrs / Semester	Marks			Duration
			Internal Assessment	Autonomous Examination	Total	
Analog and Digital Electronics Practical	5	80	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

DETAILED ALLOCATION OF MARKS

S.No	DESCRIPTION	MARKS
1	CIRCUIT DIAGRAM	25
2	CONNECTION	30
3	EXECUTION & HANDLING OF EQUIPMENT	20
4	OUTPUT /RESULT	10
5	VIVA–VOCE	5
6	MINI PROJECT	10
TOTAL		**100**

Mini Project Evaluation (10 marks)

Breakup Details

1	Project Description	05
2	Project Demo	05
	Total	**10**

COURSE DESCRIPTION:

Every Electronic Engineer should have sound knowledge about the ICs used in Electronics Industry. This is vital in R&D Department for Chip level troubleshooting. To meet the industrial needs, diploma holders must be taught about the most fundamental subject, Analog and Digital Electronics Practical. By doing practical experience in this, they will be skilled in handling all types of ICs and able to apply the skill in electronic system design and the designing of PCBs

EQUIPMENTS REQUIRED: (FOR A BATCH OF 30 STUDENTS)

S.No.	Name of the Equipments	Range	Required Nos
1	DC Regulated power supply	0-30V,1A	5
2	IC Voltage Power Supply	0-5V,1A 15-0-15V, 1A	5 5
3	Signal Generator	1MHz	4
4	Dual trace CRO	20MHz/ 30MHz	5
5	Digital Trainer	-	10
6	DC Voltmeter (Analog/Digital)	Different Ranges	5
7	DC Ammeter(Analog/Digital)	Different Range	5
8	Desk Top Computer	-	5
9	Simulation Tool	Multisim/OrCAD/ Lab view	1

OBJECTIVES:

On completion of the following experiments, the students must be able to

- Know the Verification of truth table of OR, AND, NOT, NOR, NAND, EX-OR gates.
- Know the Realization of basic gates using NAND &NOR gates.
- Know the verification of Half Adder and Full Adder using IC's.
- Know the verification of Half Subtract and Full Subtractor using IC's.
- Know the Verification of Truth Table for Decoder/Encoder.
- Know the Verification of truth table for RS, D, T&JK flip-flop.
- Test Inverting Amplifier and Non inverting amplifier using Op-amp
- Test Summing Amplifier, Difference Amplifier and Voltage Comparator using Op-amp.
- Test Integrator and Differentiator.
- Test Astable multivibrator using IC555.
- Design IC Voltage Regulator Power Supplies using IC 7805, IC7912.
- Design the PCB of 4- bit ripple counter using FF.

COURSE OUTCOMES

Course	**ECD470 Analog and Digital Electronics Practical**
After successful completion of this course, the students should be able to	
D470.1	Construct and Realize the basic gates using NAND and NOR gates, logic circuit for De-Morgan's theorems and test the performance of RS ,D,T and JK flip flop.
D470.2	Construct and test the performance of half adder, full adder, half subtractor, full subtractor Decoder/Encoder ,parity generator / checker and MUX/DEMUX
D470.3	Construct and test the performance of inverting /non inverting amplifier using OP-AMP, summing amplifier, Difference amplifier, Zero crossing detector and voltage comparator.
D470.4	Construct and test the performance of integrator and differentiator, Astable Multivibrator using IC and IC Voltage regulator using IC7805 and IC 7912.
D470.5	Practice the software tools for designing PCB of 4 bit ripple counter using FF, construct shift registers and develop the mini project with report.

ECD470 ANALOG AND DIGITAL ELECTRONICS PRACTICAL

1. Realization of basic gates using NAND &NOR gates.
2. Realization of logic circuit for De-Morgans Theorems.
3. Test the performance of Half Adder and Full Adder.
4. Test the performance of Half Subtractor and Full Subtractor.
5. Test the performance of Decoder/Encoder.
6. Test the performance of RS, D, T& JK flip-flops.
7. Test the performance of Parity generator and checker using parity checker/ generator IC's.
8. Test the performance of Multiplexer/De-multiplexer using IC4051.
9. Test the performance of Inverting Amplifier and Non inverting amplifier using Op-amp IC 741.
10. Test the performance of Summing Amplifier, Difference Amplifier.
11. Test the performance of Zero Crossing Detector and Voltage Comparator using Op- amp IC 741.
12. Test the performance of Integrator and Differentiator using Op-amp IC741.
13. Test the performance of Astable multivibrator using IC555.
14. Test the performance of IC Voltage Regulator Power Supplies using IC 7805, IC 7912.
15. Design the PCB of 4- bit ripple counter using FF using Software tool Multisim/OrCAD, Lab view.
16. Construct a 4 bit Serial in Serial out shift register and verify its functionality using simulation tools.
17. Mini Project

    The mini project is activity based and it may be given to group of maximum of six students for hands on experience and to create scientific temper

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:

a) Attendance (Award of marks same as theory courses)	:	05 Marks
b) Procedure/ observation and tabulation/ Other Practical related Work	:	05 Marks
c)Tests	:	10 Marks
d) Student Centered Learning (SCL) work sheet	:	05 Marks
Total		25 Marks

LEARNING WEBSITES

1. https://ssit.edu.in/dept/assignment/declabmanual.pdf
2. https://www.allaboutcircuits.com/video-tutorials/analog-and-digital-electronics
3. https://www.vlab.co.in/broad-area-electronics-and-communications
4. http://vlabs.iitkgp.ac.in

CO- POs & PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
D470.1	3	3	3	3	3	3	3	3	3	3
D470.2	3	3	3	3	3	3	3	3	3	3
D470.3	3	3	3	3	3	3	3	3	3	3
D470.4	3	3	3	3	3	3	3	3	3	3
D470.5	3	3	3	3	3	3	3	3	3	3
D470Total	15	15	15	15	15	15	15	15	15	15
Correlation Level	3	3	3	3	3	3	3	3	3	3

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

ECD470 ANALOG AND DIGITAL ELECTRONICS PRACTICAL

MODEL QUESTION PAPER

S.No	Experiments	CO	PO
1	Realization of basic gates using NAND & NOR gates.	D470.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
2	Realization of logic circuit for De-Morgans Theorems.	D470.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
3	Test the performance of Half Adder and Full Adder.	D470.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
4	Test the performance of Half Subtractor and Full Subtractor.	D470.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
5	Test the performance of Decoder/Encoder.	D470.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
6	Test the performance of RS, D, T & JK flip-flops.	D470.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
7	Test the performance of Parity generator and checker using parity checker/ generator IC's.	D470.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
8	Test the performance of Multiplexer/De-multiplexer using IC4051.	D470.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
9	Test the performance of Inverting Amplifier and Non inverting amplifier using Op- amp IC741.	D470.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
10	Test the performance of Summing Amplifier, Difference Amplifier.	D470.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
11	Test the performance of Zero Crossing Detector and Voltage Comparator using Op-amp IC741.	D470.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
12	Test the performance of Integrator and Differentiator using Op-amp IC741.	D470.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
13	Test the performance of Astable multivibrator using IC555.	D470.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
14	Test the performance of IC Voltage Regulator Power Supplies using IC 7805, IC 7912.	D470.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
15	Design the PCB of 4- bit ripple counter using FF using Software tool Multisim /OrCAD /Labview.	D470.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
16	Construct a 4 bit Serial in Serial out shift register and verify its functionality using simulation tools.	D470.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
17	**Mini Project**	**D470.5**	**PO1,PO2,PO3, PO4,PO5,PO6,PO7**

ECD410 INDUSTRIAL ELECTRONICS

MODEL QUESTION PAPER

Time: 3 Hrs **Max.Marks:100**

PART-A (10 X 3 = 30 Marks)					
Note: Answer all the questions. All questions carry equal marks					
S.No	Questions	UNIT	Bloom's Level	CO	PO
1	State the applications of MOSFET, GTO and IGBT.	I	R,U	D410.1	PO1,PO2
2	Explain about pulse transformer in trigger circuit.	I	R,U	D410.1	PO1,PO2
3	Define chopper and mention its uses.	II	R,U	D410.2	PO1,PO2
4	Explain natural commutation.	II	U	D410.2	PO1,PO2
5	Mention the various types of SMPS.	III	U	D410.3	PO1, PO2,PO3
6	Compare ON line UPS and OFF line UPS.	III	An	D410.3	PO1, PO2,PO3
7	State the applications of PLC.	IV	R	D410.4	PO1,PO2
8	Explain Electro-mechanical relay.	IV	U	D410.4	PO1,PO2
9	Write about Basic building blocks of Robot.	V	U	D410.5	PO4, PO5
10	Explain about direct drives.	V	U	D410.5	PO4,PO5

PART-B (5 X 14 = 70 Marks)						
Note: Answer all questions choosing A Or B in each question. All questions carry equal marks						
S.No	Questions	Marks	UNIT	Bloom's Level	CO	PO
11	(A) (i) Explain opto isolator.	07	I	U	D410.1	PO1,PO3
	(ii) Explain RC full wave firing circuit.	07	I	U	D410.1	PO1,PO3
	(OR)					
	(B) (i) Explain the operation of IGBT with neat diagram.	07	I	U	D410.1	PO1,PO3
	(ii) Explain synchronized UJT triggering circuit with the diagram.	07	1	U	D410.1	PO1,PO3
12	(A) (i) Explain the operation of single phase fully controlled bridge converter with resistive load with the diagram.	07	II	U	D410.2	PO1,PO3
	(ii) Explain commutation circuits.	07	II	U	D410.2	PO1,PO2,PO3
	(OR)					

	(B) (i) With the diagram explain the operation of Jones chopper.	07	II	U	D410.2	PO1,PO2,PO3
	(ii) Explain the principles of operation of DC chopper with diagram.	07	II	U	D410.2	PO1,PO2,PO3
13	(A).(i) Explain the various types of output voltage control used in inverters.	07	III	U	D410.3	PO1,PO3,PO4
	(ii) Explain the various types of battery banks.	07	III	U	D410.3	PO1,PO3,PO4
	(OR)					
	(B) (i) Draw the block diagram of ON line UPS and explain it.	07	III	U	D410.3	PO1,PO3,PO4
	(ii) Explain about Buck-Boost Converter.	07	III	U	D410.3	PO1,PO3,PO4
14	(A) (i) Explain the various types of arithmetic functions used in PLC.	07	IV	R	D410.4	PO3,PO4
	(ii) Draw and Explain the ladder diagram for conveyor control.	07	IV	U	D410.4	PO4,PO5
	(OR)					
	(B) (i) Explain the ladder diagram of star-delta starter.	07	IV	R	D410.4	PO4,PO5
	(ii) Draw and Explain the block diagram of PLC.	07	IV	U	D410.4	PO4,PO5
15	(A) (i) Explain the working of Robot with necessary block diagram.	07	V	R	D410.5	PO4,PO5
	(ii) Explain the working of Electric motors and its types with neat sketch.	07	V	R	D410.5	PO4,PO5
	(OR)					
	(B) (i) Explain the working of Robot sensor with neat sketch.	07	V	R	D410.5	PO4,PO5
	(ii) How sensors and actuators are being used to create self-driven vehicles?	07	V	An	D410.5	PO4,PO5

QUESTION PAPER SETTING

The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as Presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD420 COMMUNICATION ENGINEERING

MODEL QUESTION PAPER

TIME: 3hours **MARKS: 100**

PART-A (10 X 3 = 30Marks)					
Note: Answer all the questions. All questions carry equal marks.					
S.No	**Questions**	**UNIT**	**Bloom's Level**	**CO**	**PO**
1	Compare any two properties of Symmetrical and Asymmetrical networks.	I	U	D420.1	PO1,PO2
2	What are Filters? List the various types of Filters.	I	R	D420.1	PO1,PO2
3	Draw the structure of AM Wave. Indicate the various voltages present in the AM Wave.	II	U	D420.2	PO1,PO2
4	What are the advantages of SSB AM over DSB AM?	II	R	D420.2	PO1,PO2
5	Explain about frequency modulation.	III	U	D420.3	PO1,PO2
6	Differentiate between narrow band FM and Wide band FM.	III	U	D420.3	PO1,PO2
7	List the various types of pulse analog modulation techniques.	IV	R	D420.4	PO1,PO2
8	Define: (i) Quantization (ii) Nyquist rate.	IV	U	D420.4	PO1,PO2
9	Draw the structure of Composite Video signal.	V	U	D420.5	PO1,PO2
10	Define: (i) Luminance (ii) Chrominance.	V	U	D420.5	PO1,PO2

PART-B (5 X 14 = 70 Marks)						
Note: Answer all questions choosing A or B in each question. All questions carry equal marks						
S.No	**Questions**	**Marks**	**UNIT**	**Bloom's Level**	**CO**	**PO**
11	A. (i). Explain the working of Yagi- Uda antenna.	07	I	U	D420.1	PO1,PO2,PO3,PO4,PO5
	(ii). Explain the Space wave propagation.	07	I	U	D420.1	PO1,PO2
	(OR)					
	B. (i). Draw the Structure of Electromagnetic frequency spectrum with frequency band and applications of each band.	07	I	U	D420.1	PO1,PO2,PO3,PO4,PO5
	(ii). Draw the circuit diagram of Band pass filter and	07	1	U	D420.1	PO1,PO2,PO3

	explain it's working. Mention the value of its Cut-off frequencies.					
12	A. (i). Explain the working of High level AM transmitter .	07	II	U	D420.2	PO1,PO2,PO3
	(ii). Draw the frequency spectrum of AM and give the Expression for AM and AM Sidebands.	07	II	U	D420.2	PO1,PO2,PO3
	(OR)					
	B. (i). Explain the working of SSB Transmitter.	07	II	U	D420.2	PO1,PO2,PO3
	(ii) Explain the working of Super Heterodyne receiver.	07	II	U	D420.2	PO1,PO2,PO3
13	A. (i). Draw the frequency spectrum of FM. What are the effects of modulation index on frequency spectrum?	07	III	U	D420.3	PO1,PO2,PO3
	(ii). Explain the working of indirect FM transmitter.	07	III	U	D420.3	PO1,PO2,PO3
	(OR)					
	B.(i). Explain the working of Stereo phonic FM receiver.	07	III	U	D420.3	PO1,PO2,PO3
	(ii). Compare AM and FM.	07	III	U	D420.3	PO1,PO2,PO3
14	A.(i) Explain the generation of PAM. Draw its output waveform.	07	IV	U	D420.4	PO1,PO2,PO3
	(ii) Explain the working PCM Transmitter.	07	IV	U	D420.4	PO1,PO2,PO3
	(OR)					
	B.(i). Explain the working of Delta modulation. Draw its output waveform.	07	IV	U	D420.4	PO1,PO2,PO3
	(ii). Explain the Sampling and Quantization with necessary diagrams.	07	IV	U	D420.4	PO1,PO2,PO3
15	A.(i). Explain the working of Moving coil microphone.	07	V	U	D420.5	PO1,PO2,PO3
	(ii). Explain the construction and working of LED display.	07	V	U	D420.5	PO1,PO2,PO3
	(OR)					
	B. (i). Explain the working of Dynamic cone Loudspeaker.	07	V	U	D420.5	PO1,PO2,PO3
	(ii). Explain the working of PAL Colour TV receiver.	07	V	U	D420.5	PO1,PO2,PO3

QUESTION PAPER SETTING

The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as Presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD430 ANALOG AND DIGITAL ELECTRONICS

MODEL QUESTION PAPER

TIME: 3 hours MARKS: 100

PART-A (10 X 3 = 30Marks)					
Note: Answer all the questions. All questions carry equal marks					
S.No	**Questions**	**UNIT**	**Bloom's Level**	**CO**	**PO**
1	Define: CMRR.	I	R	D430.1	PO1,PO2
2	Draw the PIN diagram of OP-Amp IC 741.	I	U	D430.1	PO1,PO2
3	Differentiate between A/D Converter and D/A Converter.	II	U	D430.2	PO1,PO2
4	What are the applications of IC555?	II	U	D430.2	PO1,PO2
5	Draw the Symbol and Truth table of NOT Gate.	III	U	D430.3	PO1,PO2
6	State De-Morgan's theorems.	III	R	D430.3	PO1,PO2
7	Draw the circuit diagram of Multiplexer.	IV	U	D430.4	PO1,PO2
8	Differentiate between Encoder and Decoder.	IV	U	D430.4	PO1,PO2
9	List the various types of memories.	V	R	D430.5	PO1,PO2
10	What is flash memory?	V	R	D430.5	PO1,PO2

	PART-B (5 X 14 = 70 Marks)					
	Note: Answer all questions choosing A or B in each question. All questions carry equal marks					
S.No	**Questions**	**Marks**	**UNIT**	**Bloom's Level**	**CO**	**PO**
11	A.(i). Explain the working of Op-Amp Inverting Amplifier.	07	I	U	D430.1	PO1,PO2,PO3
	(ii). Explain the working of Zero Cross Detector.	07	I	U	D430.1	PO1,PO2,PO3
	(OR)					
	B. (i). Explain the working of Schmitt Trigger.	07	I	U	D430.1	PO1,PO2,PO3
	(ii). Draw the block diagram of Op-Amp and Draw the Symbol of Op-Amp.	07	1	U	D430.1	PO1,PO2,PO3
12	A. (i). Explain the working of IC 555 in Astable Multivibrator mode.	07	II	U	D430.2	PO1,PO2,PO3
	(ii). Explain the working of IC Voltage Regulator 78XX. What will be the values of XX.?	07	II	U	D430.2	PO1,PO2,PO3

	(OR)					
	B. (i). Explain the working of Weighted Resistor D/A Converter.	07	II	U	D430.2	PO1,PO2,PO3
	(ii) Explain the working Dual Slope A/D Converter.	07	II	U	D430.2	PO1,PO2,PO3
13	A. (i). Simplify the following logic function using K- Map $f=\sum(0,2,4,6,9,12)$.	07	III	An	D430.3	PO1,PO2,PO3
	(ii). Construct AND, NOR and EX-OR Gates using NAND Gate.	07	III	Ap	D430.3	PO1,PO2,PO3
	(OR)					
	B.(i). Reduce the following logic using K-Map. Y=ABC+ABC+ABC+ABC.	07	III	Ap	D430.3	PO1,PO2,PO3
	(ii). Convert the binary number 11001.011 into its equivalent decimal number.	07	III	Ap	D430.3	PO1,PO2,PO3
14	A.(i) Explain the working of D Flip-Flop.	07	IV	R	D430.4	PO1,PO2,PO3
	(ii) Explain the working of Serial – in –Parallel out Shift register.	07	IV	R	D430.4	PO1,PO2,PO3
	(OR)					
	B.(i). Explain the working of 3 to 8 Decoder.	07	IV	U	D430.4	PO1,PO2,PO3
	(ii).Explain the working of 8 to 1 Multiplexer.	07	IV	U	D430.4	PO1,PO2,PO3
15	A.(i).Explain RAM organization in detail with diagram.	07	V	U	D430.5	PO1,PO2,PO3
	(ii).Explain SDRAM in detail.	07	V	U	D430.5	PO1,PO2,PO3
	(OR)					
	B. (i). Explain ROM organization in detail with diagram.	07	V	U	D430.5	PO1,PO2,PO3
	(ii). Explain anti fuse technologies.	07	V	U	D430.5	PO1,PO2,PO3

QUESTION PAPER SETTING

The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as Presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD440 E VEHICLE TECHNOLOGY & POLICY

MODEL QUESTION PAPER

Time: 3 Hrs Max.Marks:100

PART-A (10 X 3 = 30Marks)					
Note: Answer all the questions. All questions carry equal marks					
S.No	**Questions**	**UNIT**	**Bloom's Level**	**CO**	**PO**
1	What is the Parts of Drive train system?	I	R	D440.1	PO1,PO2
2	Draw the block diagram of BEV.	I	U	D440.1	PO1,PO2
3	Define energy consumption.	II	R	D440.2	PO1,PO2
4	What are the types of EV motors?	II	R	D440.2	PO1,PO2
5	What is Electrochemical Batteries?	III	R	D440.3	PO1,PO2
6	Explain Nickel Based Batteries.	III	U	D440.3	PO1,PO2
7	What is Global Scenario of EV adoption?	IV	R	D440.4	PO1,PO2
8	Explain about AIS 038.	IV	U	D440.4	PO1,PO2
9	What is Policy Measures?	V	R	D440.5	PO1,PO2
10	Explain Recycling Ecosystem.	V	U	D440.5	PO1,PO2

PART-B (5 X 14 = 70 Marks)						
Note: Answer all questions choosing A or B in each question. All questions carry equal marks						
S.No	**Questions**	**Marks**	**UNIT**	**Bloom's Level**	**CO**	**PO**
11	(A) (i) Explain about Rear Wheel, Front Wheel and All wheel.	07	I	U	D440.1	PO1,PO2,PO3,PO4,PO5
	(ii) Explain about the Parts of Drive train system.	07	I	U	D440.1	PO1,PO2,PO3,PO4,PO5
	(OR)					
	(B) (i) Explain about Hybrid electric Vehicle (HEV).	07	I	U	D440.1	PO1,PO2,PO3,PO4,PO5
	(ii) Explain about Plug-in Hybrid Electric Vehicle (PHEV).	07	1	U	D440.1	PO1,PO2,PO3,PO4,PO5
12	(A) (i) What is the Concept of Hybrid electric drive trains?	07	II	U	D440.2	PO1,PO2,PO3,PO4,PO5
	(ii) Explain Series, Parallel and Series & Parallel.	07	II	U	D440.2	PO1,PO2,PO3

	(OR)					
	(B) (i) Briefly explain about Permanent Magnetic Brush Less DC Motor Drives (BLDC).	07	II	U	D440.2	PO1,PO2,PO3
	(ii) What are the Merits and Demerits of DC motor drive?	07	II	U	D440.2	PO1,PO2,PO3
13	(A).(i) Explain the Construction and working of Lead Acid Batteries.	07	III	U	D440.3	PO1,PO2,PO3
	(ii) Explain the Lithium Based Batteries Role of Battery Management System (BMS).	07	III	U	D440.3	PO1,PO2,PO3
	(OR)					
	(B) (i) Explain the Latest development in battery chemistry.	07	III	U	D440.3	PO1,PO2,PO3
	(ii) Explain the Impacts on Environment – Impacts on Economy.	07	III	U	D440.3	PO1,PO2,PO3
14	(A) (i) Explain about Government of India Electric Mobility Policy Frame work.	07	IV	U	D440.4	PO1,PO3,PO5
	(ii) Explain the National Electric Mobility Mission Plan 2020.	07	IV	U	D440.4	PO1,PO3,PO5
	(OR)					
	(B) (i) Explain the Scope and Applicability of EV Policy.	07	IV	U	D440.4	PO1,PO3,PO5
	(ii) Explain the ARAI Standards for Electric Vehicle.	07	IV	U	D440.4	PO1,PO3,PO5
15	(A) (i) Briefly explain about Tamil Nadu E-vehicle Policy 2019.	07	V	U	D440.5	PO1,PO3,PO5
	(ii) Explain Demand side incentives.	07	V	U	D440.5	PO1,PO3,PO5
	(OR)					
	(B) (i) Explain the Revision of Transport Regulation of EV.	07	V	U	D440.5	PO1,PO3,PO5
	(ii) Explain and details of R&D and Business Incubation .	07	V	U	D440.5	PO1,PO3,PO5

QUESTION PAPER SETTING

The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as Presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD510 ANALOG AND DIGITAL COMMUNICATION SYSTEMS

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 16 weeks

Course	Instruction		Examination			
			Marks			
Analog and Digital Communication Systems	**Hrs/ Week**	**Hrs/ Semester**	**Internal Assessment**	**Autonomous Examination**	**Total**	**Duration**
	5	80	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

TOPICS AND ALLOCATION OF HOURS:

UNIT	TOPICS	NO.OF HOURS
I	Radar, Navigational Aids, Telephony	14
II	Digital Communication	14
III	Optical Communication	14
IV	Satellite Communication	14
V	Mobile Communication	15
Tests and Model Exam		9
TOTAL		**80**

COURSE DESCRIPTION:

The course Analog and Digital communication systems will enable the students to learn about the advancement in communication systems. It will give exposure to the various modes of communication viz Radar, Telephone, digital communication, digital codes, optical communication, satellite communication, microwave communication, mobile communication and satellite multiple access techniques.

OBJECTIVES:

On completion of the following units of syllabus contents, the students should be able to:

- Understand principles of Radar.
- Understand principles of navigational aids.
- Study Electronic Exchange.
- Study basic digital communication system and discuss the characteristics of data transmission circuits.

- Learn Error detection and correction codes and various digital modulation techniques.
- Learn optical sources, optical detectors.
- Discuss the applications of fiber optic communication.
- Study satellite system, orbits, launching, Antennas.
- Study earth segment and space segment components .
- Study about satellite services.
- Study fundamental cellular concepts such as frequency reuse ,hand off.
- Learn multiple access techniques.
- Learn digital cellular system-GSM.

COURSE OUTCOMES

Course	**ECD510 ANALOG AND DIGITAL COMMUNICATION SYSTEMS**
After successful completion of this course, the students should be able to	
D510.1	Understand the fundamentals of RADAR and Telephony .
D510.2	Learn about basics of Digital communication systems and digital codes
D510.3	Acquire knowledge on Optical communication systems, losses, optical sources and applications.
D510.4	Understand about Satellite communication and Microwave communication systems
D510.5	Familiarize about Mobile communication and multiple access techniques.

ECD510 ANALOG AND DIGITAL COMMUNICATION SYSTEMS

UNIT – I

RADAR AND NAVIGATIONAL AIDS **[14Hrs]**

1.1 RADAR

Basic Radar System– Applications [1 Hr]

Radar Range Equation(Qualitative Treatment Only) [1 Hr]

Factors Influencing Maximum Range [1 Hr]

Basic Pulsed Radar System – Block Diagram [2 Hrs]

Display Methods- A - Scope, PPI Display - Instrument Landing System [1 Hr]

Ground Controlled Approach System [1 Hr]

1.2 TELEPHONY

Telephone System–Public Switched Telephone Network (PSTN) [2 Hrs]

Electronic Switching System – Block Diagram [2 Hrs]

ISDN –Architecture, Features [2 Hrs]

Video Phone– Block Diagram. [1 Hr]

UNIT-II

DIGITAL COMMUNICATION **[14Hrs]**

2.1 BASICS OF DIGITAL COMMUNICATION SYSTEM:

Basic Elements of Digital Communication System [1 Hr]

Block Diagram- Characteristics of Data Transmission Circuits [2 Hrs]

Bandwidth Requirement – Speed – Baud Rate – Noise -Crosstalk – Distortion [2 Hrs]

2.2 DIGITAL CODES:

ASCII Code – EBCDIC Code – Error Detection Codes [2 Hrs]

Parity Check Codes – Redundant Codes – Error Correction Codes [2 Hrs]

Retransmission- Forward Error Correcting Code – Hamming Code

Digital Modulation Techniques [2 Hrs]

ASK, FSK, PSK, QPSK Modulation/Demodulation Techniques(Only Block Diagram And Operation) [3 Hrs]

UNIT-III

OPTICAL COMMUNICATION **[14Hrs]**

3.1 BASICS OF OPTICAL COMMUNICATION AND LOSSES:

Optical Communication System – Block Diagram [1 Hr]

Advantages of Optical Fiber Communication Systems [1 Hr]

Principles of Light Transmission in a Fiber Using Ray Theory [1 Hr]

Single Mode Fibers, Multimode Fibers [1 Hr]

Step Index Fibers, Graded Index Fibers (Basic Concepts Only) [1 Hr]

Attenuation In Optical Fibers –Absorption Losses, Scattering Losses [1 Hr]

Bending Losses, Core and Cladding Losses. [1 Hr]

3.2 OPTICAL SOURCES AND APPLICATIONS:

Optical Sources – LED – Semiconductor LASER – Principles [1 Hr]

Optical Detectors – PIN and APD Diodes [2 Hrs]

Optical Transmitter – Block Diagram [1 Hr]

Optical Receiver – Block Diagram [1 Hr]

Application of Optical Fibers – Networking, Industry and Military Applications. [2 Hrs]

UNIT-IV

SATELLITE COMMUNICATION **[14Hrs]**

4.1 SATELLITE SYSTEM:

Kepler's I,II,II laws – orbits – launching orbits types [1 Hr]

Geostationary synchronous satellites-Advantages [1 Hr]

Apogee Perigee - Active and passive satellite - Earth eclipse of satellite. [1 Hr]

4.2 ANTENNA:

Parabolic reflector antenna. [1 Hr]

4.3 SPACE SEGMENT:

Space segment: Power supply [1 Hr]

Attitude control- station keeping [1 Hr]

Transponders – TT and C subsystem – Antenna subsystem [1 Hr]

4.4 EARTH SEGMENT:

Earth segment: Block diagram of Transmit receive earth station [2 Hrs]

Satellite mobile services - Basics of GPS. [1 Hr]

4.5 MICROWAVE COMMUNICATION:

Microwave frequency ranges microwave devices [1 Hr]

Parametric amplifiers – Travelling wave tubes [1 Hr]

Simple block diagram of Microwave Transmitter, Receiver [1 Hr]

and Microwave link repeater. [1 Hr]

UNIT V

MOBILE COMMUNICATION AND MUTIPLE ACCESS TECHNIQUES [15Hrs]

5.1 MOBILE COMMUNICATION:(Qualitative Treatment only)

Cellular telephone–fundamental concepts [1 Hr]

Simplified Cellular telephone system - frequency reuse [1 Hr]

Interference – Co-channel Interference – Adjacent Channel Interference [2 Hrs]

Improving coverage and capacity in cellular systems [1 Hr]

cell splitting – sectoring – Roaming and Handoff – Basics of blue tooth technology. [2 Hrs]

Development of wireless network-3G,4G,5G [1 Hr]

5.2 SATELLITE MULTIPLE ACCESS TECHNIQUES:

TDMA, FDMA,CDMA. [2 Hrs]

Digital cellular system [1 Hr]

Global system for mobile communications (GSM) –GSM services [2 Hrs]

GSM System Architecture – Basics of GPRS. [2 Hrs]

Tests & Model Exam [9 Hrs]

TEXT BOOKS:

S.NO	TITLE	AUTHOR	PUBLISHER WITH EDITION
1.	Electronic communication systems	Kennedy& Davis	Tata McGraw Publication Fourth Edition 1999
2.	Electronics communication	Dennis Roddy and John coolen	PHI , Third Edition,1988

REFERENCE BOOKS:

S.NO	TITLE	AUTHOR	PUBLISHER WITH EDITION
1.	Optical fiber communication	Gerd Keiser	Tata McGraw Hill Publication , Third Edition ,2000
2.	Satellite communication	Dr. D.C.	Khanna publishers ,Third Edition ,1995

		Agarwal	
3.	Satellite communication	Dennis Roddy	Tata McGraw Hill publication, Third Edition 2010
4.	Electronic communication systems- Fundamentals through Advanced	Wayne Tomasi	Pearson Education Fifth Edition 2005

LEARNING WEBSITES

1. https://byjus.com/physics/satellite-communication/
2. https://www.tutorialspoint.com/analog_communication/index.htm
3. https://www.allaboutcircuits.com/textbook/digital/chpt-14/optical-data-communication/
4. https://learn.sparkfun.com/tutorials/analog-vs-digital/all
5. https://www.pdfdrive.com/an-introduction-to-analog-and-digital-communications-2nd-d18457332.html

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	-	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
D510.1	3	3	3	3	3	2	2	3	2	2
D510.2	3	3	3	3	3	2	2	3	2	2
D510.3	3	3	3	3	3	2	2	3	2	2
D510.4	3	3	3	3	3	2	2	3	2	2
D510.5	3	3	3	3	3	2	2	3	2	2
D510Total	15	15	15	15	15	10	10	15	10	10
Correlation Level	3	3	3	3	3	2	2	3	2	2

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD520 MICROCONTROLLER AND ITS APPLICATIONS

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 16 weeks

Course	Instructions		Examination			
			Marks			
Microcontroller and its Applications	**Hrs/ Week**	**Hrs/ Semester**	**Internal Assessment**	**Autonomous Examination**	**Total**	**Duration**
	5	80	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

TOPICS AND ALLOCATION:

UNIT	TOPICS	NO.OF HOURS
I	Architecture of 8051 Microcontroller	15
II	8051 Instruction set and Programming	15
III	Peripherals of 8051	15
IV	Interfacing techniques	15
V	Advanced Microcontrollers	11
	Tests& Model Exam	9
TOTAL		80

COURSE DESCRIPTION:

The introduction of this course will enable the students to learn about microcontroller 8051 architecture, Pin details, Instruction sets, Programming and interfacing. This subject enables the students to do the project effectively. It also helps the students to choose the field of interest. If the student is aiming for higher studies, this subject is foundation

OBJECTIVES:

On successful completion of the course, the students must be able to

- Know the difference between microprocessor and microcontroller.
- Understand the architecture of 8051.
- Write programs using 8051 ALP.
- Understand the programming of I/O ports, Timer, Interrupt and Serial Programming.
- Use the interfacing techniques.
- Know the types of microcontrollers.
- Explain IoT.

COURSE OUTCOMES

Course	**ECD520 MICROCONTROLLER AND ITS APPLICATIONS**
After successful completion of this course, the students should be able to	
D520.1	Understand the architecture of microcontroller 8051.
D520.2	Analyze the instruction set of 8051 microcontroller and write assembly language programs.
D520.3	Understand I/O ports, Timer and Counter programming, serial communication and Interrupts.
D520.4	Familiarize about the interfacing techniques of 8051 with 8255.
D520.5	Understand the types of microcontroller and IoT.

ECD520 MICROCONTROLLER AND ITS APPLICATIONS

UNIT I

ARCHITECTURE OF 8051 MICROCONTROLLER **[15 Hrs]**

ARCHITECTURE:

Microprocessor-Microcontroller [1 Hr]

Comparison of microprocessor and microcontroller [1 Hr]

Architecture diagram of microcontroller 8051 [1 Hr]

Functions of each block- [1 Hr]

Pin details of 8051-ALU- ROM-RAM- [1 Hr]

Memory organization of 8051- [1 Hr]

Special function registers-Program counter- [2 Hrs]

PSW register-Stack- I/O ports-Timer [1 Hr]

Interrupt-serial port-External memory- [1 Hr]

Oscillator and Clock-Reset-Power on reset- [2 Hrs]

Clock cycle-machine cycle-Instruction cycle- [2 Hrs]

Overview of 8051 family. [1Hr]

UNIT II

8051 INSTRUCTION SET AND PROGRAMMING **[15 Hrs]**

2.1 INSTRUCTION SET OF 8051

Instruction set of 8051- [1 Hr]

Classification of 8051 instructions-data transfer instructions- [1 Hr]

Arithmetic instructions-Logical instructions-Branching instructions [2 Hrs]

-Bit manipulation instructions- [1 Hr]

Assembling and running an 8051 program- [1 Hr]

Structure of Assembly language-Assembler directives- [1 Hr]

Different Addressing modes of 8051-Time delay routines. [1 Hr]

2.2 ASSEMBLY LANGUAGE PROGRAMS:

16 bit addition and 16 bit subtraction- [2 Hrs]

8 bit multiplication and 8 bit division [2 Hrs]

BCD to HEX code conversion-HEX to BCD code conversion. [2 Hrs]

Smallest number/ Biggest number. [1 Hr]

UNIT III

PERIPHERALS OF 8051 **[15 Hrs]**

3.1 I/O PORTS:

Bit addresses for I/O ports-I/O port programming- [2 Hrs]

I/O bit manipulation programming. [2 Hrs]

3.2 TIMER/COUNTER :

SFRS for Timer- Modes of Timers/counters [2 Hrs]

Programming 8051 Timer(Simple programs) [2 Hrs]

3.3 SERIAL COMMUNICATION:

Basics of serial communication- [1 Hr]

SFRs for serial communication-RS232 standard- [2 Hrs]

8051 connection to RS 232-8051 serial port programming. [2 Hrs]

Interrupts: 8051 interrupts- SFRs for interrupt-Interrupt priority. [2 Hrs]

UNIT IV

INTERFACING TECHNIQUES **[15 Hrs]**

4.1 IC 8255:

IC 8255-Block diagram- [2 Hrs]

Modes of 8255-8051 interfacing with 8255 [1 Hr]

4.2 INTERFACING:

Interfacing external memory to 8051- [1 Hr]

Relay interfacing Sensor interfacing [2 Hrs]

Seven segment LED display interfacing- [2 Hrs]

Keyboard interfacing-Stepper motor interfacing- [2 Hrs]

ADC Interfacing- [2 Hrs]

DAC interfacing- [2 Hrs]

DC motor interfacing using PWM-LCD interfacing [1 Hr]

UNIT V [**11 Hrs**]

ADVANCED MICROCONTROLLERS :

5.1 TYPES OF MICROCONTROLLERS: [2 Hrs]

PIC microcontroller-General Block diagram-Features-Applications- [2 Hrs]

Arduino- General Block diagram-Variants-Features-Applications- [2 Hrs]

Raspberry pi-General Block diagram-Features-Applications- [2 Hrs]

Comparison of microcontrollers.

5.2 IoT:

Introduction to IoT-Block diagram of home automation using IoT- [2 Hrs]

IoT applications [1Hr]

Tests and Model Exams **[9 Hrs]**

TEXT BOOKS:

S.No	Title	Author	Publisher with edition
1.	Microcontrollers, Principles and Applications	Ajit pal	PHI Ltd,-2011
2.	8051 Microcontroller and Embedded Systems using Assembly and C	Mazidi and D.MacKinlay	Pearson Education-2006

REFERENCE BOOKS:

S.No	Title	Author	Publisher with edition
1.	Microprocessor and Microcontroller	R. Theagarajan	Sci Tech Publication, Chennai.
2.	Design with PIC micro controllers	J.B. Peatman	Pearson Education India
3.	Beginning Arduino	Michael McRoberts	Apress
4.	Getting started with RaspberryPi	Matt Richardson	Maker media incorporated
5.	The Internet of Things	Samuel Greengard	MIT Press

LEARNING WEBSITES

1. https://www.electronicshub.org/microcontrollers/
2. https://www.electricaltechnology.org/2020/05/types-of-microcontrollers.html
3. https://www.codrey.com/learn/microcontroller-basics/

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
D520.1	3	3	2	2	2	2	2	3	2	2
D520.2	3	3	2	2	2	2	2	3	2	2
D520.3	3	3	2	2	2	2	2	3	2	2
D520.4	3	3	2	2	2	2	2	3	2	2
D520.5	3	3	2	2	2	2	2	3	2	2
D520Total	15	15	10	10	10	10	10	15	10	10
Correlation Level	3	3	2	2	2	2	2	3	2	2

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
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% to be included	90%	10%

****

ECD531 VERY LARGE SCALE INTEGRATION

TEACHING AND SCHEME OF EXAMINATION:

No. of weeks per semester: 16 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/ Week	Hrs / Semester	Internal Assessment	Autonomous Examination	Total	
Very Large Scale Integration	4	64	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

TOPICS AND ALLOCATION OF HOURS:

UNIT	TOPICS	NO. OF HOURS
I	Introduction to VLSI	11
II	Introduction to VHDL	10
III	Combinational Circuit Design	11
IV	Sequential Circuit Design	12
V	Programmable Logic Devices	11
	Tests& Model Exam	9
TOTAL		**64**

COURSE DESCRIPTION:

Very Large Scale Integration technology, when especially used for designing digital systems, it is mandatory that the behavior of the required system to be described (modeled) and verified (simulated) before synthesis, translate the design into real hardware fabrication in the foundry (gates and wires).Hardware Description Language (HDL) allows designs to be described using any methodology-top down, bottom up approach. VHDL can be used to describe hardware at the gate level or in a more abstract way. This course is to introduce the digital system design concepts through hardware description Language, VHDL programming, design flow of VLSI and architectures of CPLD, FPGA. It is mainly aimed at design of combinational and sequential functions and simulates or verifies their functionality using the Hardware description Language (HDL).

OBJECTIVES:

At the end of the Course, the students will be able to

- Understand the concepts of VLSI design process.
- Develop a VHDL code for combinational circuit
- Develop a VHDL code for sequential circuit.
- Explain the importance of PROM, PLA, and PAL.
- Differentiate PROM, PLA and PAL.
- Develop the circuit using PROM ,PAL and PLA.
- Understand CPLD and FPGA hardware.
- Differentiate ASIC, CPLD,FPGA.

COURSE OUTCOMES

Course	**ECD531 VERY LARGE SCALE INTEGRATION**
After successful completion of this course, the students should be able to	
D531.1	Understand the NMOS, CMOS Logic and VLSI Design Process.
D531.2	Familiarize about VHDL program format, VHDL statements and develop VHDL codes for Logic circuits.
D531.3	Analyse the Combinational circuit design and develop VHDL programs for combinational circuit
D531.4	Analyse the sequential circuit and Develop VHDL programs for Sequential Circuits
D531.5	Know the Programmable Logic Devices like PROM,PLA,PAL,CPLD,FPGA and ASIC

ECD531 VERY LARGE SCALE INTEGRATION

UNIT I

INTRODUCTION TO VLSI: **[11Hrs]**

1.1 NMOS ,CMOS LOGIC:

NOT, AND, OR, NAND, and [1 Hr]

NOR Gates using NMOS – [1 Hr]

NOT, AND, [1 Hr]

OR, NAND, and [1 Hr]

NOR Gates using CMOS – [1 Hr]

Implementation of logic function (SOP, POS) in CMOS. [1 Hr]

1.2 VLSI DESIGN PROCESS:

Different level of abstractions in VLSI design [1 Hr]

steps involved in VLSI design process: [1 Hr]

Design Entry, Simulation, Synthesis, [1 Hr]

Placement and Routing Layout rules, [1 Hr]

Stick diagram. [1 Hr]

UNIT II

INTRODUCTION TO VHDL **[10 Hrs]**

2.1 INTRODUCTION:

VHDL – Different types of modeling – [1 Hr]

General format for VHDL program . [1 Hr]

2.2 VHDL STATEMENTS:

Syntax for process statement, if statement, [1 Hr]

if else statement, if else if else statement case statement – [1 Hr]

Syntax for signal declaration and signal assignment statement – [1 Hr]

Syntax for variable declaration and variable assignment statement, [1 Hr]

component declaration.

2.3 VHDL CODE EXAMPLE:

VHDL code for Logic gates [1 Hr]

AND, OR, NOT, [1 Hr]

NAND, NOR gate [1 Hr]

and XOR gates. [1 Hr]

UNIT III

COMBINATIONAL CIRCUIT DESIGN [11 Hrs]

3.1 COMBINATIONAL CIRCUIT:

Half adder, Full adder, [1 Hr]

Half subtractor and Full subtractor – [1 Hr]

4 to 1 Mux, 1 to 4 Demux, [1 Hr]

4 to 2 Encoder, 2 to 4 decoder and comparator [1 Hr]

– Four bit Arithmetic adder – [1 Hr]

Four bit Arithmetic subtractor [1 Hr]

3.2 VHDL PROGRAM FOR COMBINATIONAL CIRCUIT:

VHDL program for Half adder, Full adder – [1 Hr]

VHDL program for Half subtractor and Full subtractor – [1 Hr]

4 to 1 Mux, 1 to 4 Demux, [1 Hr]

4 to 2 Encoder, 2 to 4 decoder and comparator in VHDL – [1 Hr]

VHDL program for Four bit Arithmetic adder (structural) – [1 Hr]

VHDL program for Four bit Arithmetic subtractor (structural)

UNIT IV

SEQUENTIAL CIRCUIT DESIGN [12Hrs]

4.1SEQUENTIALCIRCUIT:

Flip-flops: D,JK and [1 Hr]

T Flip-flops – [1 Hr]

counters:3 bit up Counter,3 bit down counter and [1 Hr]

3 bit up/down counter, Decade counter, [2 Hrs]

ring counter and Johnson Counter. [1 Hr]

4.2VHDL PROGRAM FOR SEQUENTIAL CIRCUIT:

VHDL program for D, JK and T FlipFlops [1 Hr]

with reset input, without reset input– [1 Hr]

VHDL program for 3 bit up Counter [1 Hr]

3 bit down counter and 3 bit up/down counter, [1 Hr]

VHDL program for serial adder [1 Hr]

Decade counter, ring counter and Johnson Counter [1 Hr]

UNIT V

PROGRAMMABLE LOGIC DEVICES [11 Hrs]

5.1 PROM, PLA AND PAL :

Introduction to PROM, PLA and PAL [1Hr]

Implementation of combinational [2Hrs]

circuits with PROM, PAL and PLA(upto 4variables) – [1Hr]

Comparison between PROM, PAL and PLA [1Hr]

5.2 CPLD,FPGA AND ASIC :

Architecture of Complex Programmable Logic device (CPLD) – [2Hrs]

Architecture of Field Programmable Gate Arrays(FPGA) – [2Hrs]

Introduction to Application Specific Integrated Circuit(ASIC) – [1Hr]

Types Of ASIC – ASIC design flow [1Hr]

Tests & Model Exam [**9 Hrs]**

TEXT BOOKS:

S.No	Title	Author	Publisher with Edition
1.	Digital Design	M.Morris Mano ,Michael D Ciletti	Pearson Education2008.
2.	VHDL Prime	Bhasker J	Prentice Hall India-2009

REFERENCE BOOKS:

S.No	Title	Author	Publisher with Edition
1.	Principles of CMOS VLSI design	NEIL H.E.WESTE, KAMRAN ESRHAGHIAN	Wesley professional, second edition1994
2.	Digital Electronics with PLD Integration	Nigel P. Cook	Pearson 2000.
3.	Programmable Logic Handbook: PLDs ,CPLDs ,and FPGAs	Ashok K. Sharma	TATA Mcgraw-Hill,1998
4.	Application Specific Integrated Circuits	Michael John Sebastian Smith	Addison- Wesley Professional first edition 1997

LEARNING WEBSITES

1. https://www.britannica.com/technology/very-large-scale-integration
2. https://www.sciencedirect.com/topics/computer-science/very-large-scale-integration
3. https://engineeringbookspdf.com/digital-integrated-circuit-design-from-vlsi-architectures-to-cmos-fabrication-pdf-free-download

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
D531.1	3	3	2	2	2	2	2	3	3	3
D531.2	3	3	2	2	2	2	2	3	3	3
D531.3	3	3	2	2	2	2	2	3	3	3
D531.4	3	3	2	2	2	2	2	3	3	3
D531.5	3	3	2	2	2	2	2	3	3	3
D531Total	15	15	10	10	10	10	10	15	15	15
Correlation Level	3	3	2	2	2	2	2	3	3	3

Correlation level 1- Slight (low)
Correlation level 2- Moderate (Medium)
Correlation level 3- Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap -Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD532 CONSUMER ELECTRONICS

TEACHING AND SCHEME OF EXAMINATION:

No. of weeks per semester: 16 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/ Week	Hrs / Semester	Internal Assessment	Autonomous Examination	Total	
Consumer Electronics	4	64	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

TOPICS AND ALLOCATION OF HOURS:

UNIT	TOPICS	NO. OF HOURS
I	Audio system	11
II	Audio recording and reproducing system	12
III	Colour TV	11
IV	Digital Transmission and reception	11
V	Consumer Appliances	10
	Tests & Model Exam	9
TOTAL		**64**

COURSE DESCRIPTION:

The objective of teaching this course is to give students in depth knowledge of various electronic audio and video devices and systems. Further, this subject will introduce the students with working principles, block diagram, main features of consumer electronics Gadgets/goods/devices. This in-turn will develop in them capabilities of assembling, fault Diagnosis and rectification in a systematic way.

OBJECTIVES:

On Successful Completion at the end of the Course, the students will be able to

- Understand the various types of microphones and loudspeakers.
- To identify the various digital and analog signal.
- Describe the basis of television and composite video signal.
- Describe the various kinds of colour TV standards and system.

- Compare the various types of digital TV system.
- Understand the various types of consumer goods.
- Maintain various consumer electronic appliances.

COURSE OUTCOMES

Course	**ECD532 CONSUMER ELECTRONICS**
After successful completion of this course, the students should be able to	
D532.1	Understand the basics of audio system and different types of sound recording .
D532.2	Familiarize about sound reproducing systems and different types audio recording systems
D532.3	Know the fundamentals of colour TV and TV encoders..
D532.4	Understand the fundamentals of Digital transmission and reception
D532.5	Understand the basic principle and working of various consumer appliances.

ECD532 CONSUMER ELECTRONICS

UNIT I

INTRODUCTION TO AUDIO SYSTEM **[11 Hrs]**

1.1 AUDIOSYSTEM:

Microphones and Loudspeakers: [1 Hr]

Carbon, moving coil, [1 Hr]

cordless microphone, [1 Hr]

Direct radiating and [1 Hr]

horn loudspeaker, [1 Hr]

Multi-speaker system. [1 Hr]

1.2 SOUND RECORDING:

Magnetic Recording, [2 Hrs]

Digital Recording, [2 Hrs]

Optical Recording (CD system, DVD, Blu-ray Disc) [1 Hr]

UNIT II

AUDIO REPRODUCING SYSTEM AND RECORDING **[12 Hrs]**

2.1 REPRODUCING SYSTEM

Sound reproducing Systems: Monophonic, Stereophonic, [2 Hrs]

Surround System, Hi-Fi system, [2 Hrs]

block diagram and use of Home Theatre Systems. [2 Hrs]

2.2 AUDIO RECORDING:

SOUND RECORDING: PRINCIPLES OF SOUND RECORDING:

Magnetic Recording/ Reproduction. [2 Hrs]

Audio CD Recording/ Reproduction, [2 Hrs]

Study of working principle of audio and VCD, [1 Hr]

Digital sound recording on CD system, MP3. [1 Hr]

UNIT III

COLOUR TV **[11 Hrs]**

3.1 COLOUR TV:

Primary colours, concepts of additive and subtracting [1 Hr]

mixing of colours, concepts of luminance, [2 Hrs]

Hue and Saturation, Representation of a colour in colour triangle, [1 Hr]

non-spectral colour, visibility curve. [1 Hr]

3.2 TV ENCODERS:

Compatibility of colour TV system with monochrome system. [2 Hrs]

Basic colour TV system-NTSC, SECAM, and PAL their advantages and disadvantages. [2 Hrs]

Construction and working principles of Trinitron and PIL types of colour picture tubes. [2 Hrs]

UNIT IV

DIGITAL TRANSMISSION AND RECEPTION [11 Hrs]

4.1 DIGITAL TRANSMISSION:

Digital satellite television, [2 Hrs]

Direct-To-Home (DTH) satellite television, [2 Hrs]

Introduction to: Video on demand, CCTV, [1 Hr]

High Definition (HD)-TV [1 Hr]

4.2 RECEPTION:

Introduction to Liquid Crystal and LED Screen Televisions [2 Hrs]

Basic block diagram of LCD and [2 Hrs]

LED Television and their comparison. [1 Hr]

UNIT V

CONSUMER APPLIANCES: [10 Hrs]

Basics principle and working of Microwave Oven, [2Hrs]

Photostat Machine [2Hrs]

and Digital Camera, [1Hrs]

Camcorder Washing Machine: [1Hrs]

wiring diagram, electronic controller for washing machine, [2Hrs]

technical specifications, types of washing machine, fuzzy logic. [2Hrs]

Tests & Model Exam [9 Hrs]

TEXT BOOKS:

S.No	Title	Author	Publisher with Edition
1.	Consumer Electronics	Bali S.P	Pearson Education 2010.
2.	Colour TV	A.Dhake	Tata McGraw-Hill Education

REFERENCE BOOKS:

S.No	Title	Author	Publisher with Edition
1.	Audio Video Systems	R. G. Gupta	McGraw Hill Education System
2.	Consumer Electronics	Yagnik & Jain	Ishan Publication

LEARNING WEBSITES:

1. https://www.semtech.com/applications/consumer-electronics
2. https://www.sciencedirect.com/topics/engineering/consumer-electronics
3. https://www.pdfdrive.com/consumer-electronics-troubleshooting-and-repair-handbook-e161161617.html

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO-POs & PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
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D532.3	3	3	3	3	3	2	2	2	2	2
D532.4	3	3	3	3	3	2	2	2	2	2
D532.5	3	3	3	3	3	2	2	2	2	2
D532 Total	15	15	15	15	15	10	10	10	10	10
Correlation Level	3	3	3	3	3	2	2	2	2	2

Correlation level 1- Slight (low)
Correlation level 2- Moderate (Medium)
Correlation level 3- Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD533 BASICS OF DIGITAL SIGNAL AND IMAGE PROCESSING

TEACHING AND SCHEME OF EXAMINATION:

No. of weeks per semester: 16 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/ Week	Hrs / Semester	Internal Assessment	Autonomous Examination	Total	
Basics of Digital Image Processing	4	64	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

TOPICS AND ALLOCATION OF HOURS:

UNIT	TOPICS	NO. OF HOURS
I	Classification of Signals and systems	10
II	Analysis of continuous time Signals	12
III	Digital Image Fundamentals	10
IV	Image Enhancement and Image Restoration	12
V	Image Segmentation and compression	11
	Tests& Model Exam	9
	TOTAL	**64**

COURSE DESCRIPTION:

The course basic of digital signal and image processing introduce visualization and mathematical representation of continuous time and discrete time signals and ability to analyses LTI system and give clear explanation of image compression, restoration, enhancement, segmentation. The student will have depth of knowledge about signal and image processing which will help in industries and in bio medical field.

OBJECTIVES:

On Successful completion at the end of the Course, the students will be able to

- Know about basic knowledge of signals and system.
- Know fourier representation of periodic signals.
- Be able to characterize LTI system.
- Steps in image processing.
- Simple image fundamental.
- Various image enhancement techniques.

- Histogram processing.
- Spatial filtering.
- Understand various compression models.
- Study JPEG techniques.
- Detection of point, line, edge in images.

COURSE OUTCOMES

Course	**ECD533 BASICS OF DIGITAL SIGNAL AND IMAGE PROCESSING**
After successful completion of this course, the students should be able to	
D533.1	Understand the classification of signals and systems.
D533.2	Analyse the Continuous Time signals Fourier and Laplace Transforms.
D533.3	Understand basics of image processing ,Image sampling ,quantization and colour image fundamentals
D533.4	Learn about image enhancement and image restoration.
D533.5	Understand the image segmentation and image compression.

ECD533 BASICS OF DIGITAL SIGNAL AND IMAGE PROCESSING

UNIT- I

CLASSIFICATION OF SIGNALS AND SYSTEMS **[10 Hrs]**

1.1 SIGNALS:

Standard signals-Step, Ramp, Pulse, Impulse, [1 Hr]

Real and complex exponentials and Sinusoids- [1 Hr]

Classification of signals – Continuous time (CT) and Discrete [1 Hr]

Time (DT) signals, Periodic & Aperiodic signals, [1 Hr]

Deterministic & Random signals, Energy & Power signals [1 Hr]

1.2 SYSTEMS:

Classification of systems- CT systems and DT systems- [2 Hrs]

Linear & Nonlinear, Time-variant & Time-invariant, [2 Hrs]

Causal & Non-causal, Stable & Unstable. [1 Hr]

UNIT- II

ANALYSIS OF CONTINUOUS TIME SIGNAL **[12 Hrs]**

2.1 FOURIER TRANSFORM:

Fourier series for periodic signals [3 Hrs]

Fourier Transform – [2 Hrs]

properties [2 Hrs]

2.2 LAPLACE TRANSFORM:

Laplace Transforms [3 Hrs]

Laplace Transforms properties [2 Hrs]

UNIT-III

DIGITAL IMAGE FUNDAMENTALS **[10 Hrs]**

3.1 BASICS OF IMAGE PROCESSING:

Steps in Digital Image Processing– [2 Hrs]

Components–Elements of Visual Perception – [2 Hrs]

Image Sensing and Acquisition – [1 Hr]

Relationships between pixels [1 Hr]

3.2 IMAGE SAMPLING AND QUANTIZATION [2 Hrs]

3.3 COLOR IMAGE FUNDAMENTALS:

RGB,HSI models**.** [2 Hrs]

UNIT-IV

IMAGE ENHANCEMENT AND IMAGE RESTORATION **[12 Hrs]**

4.1 IMAGE ENHANCEMENT:

Spatial Domain: Gray level transformations– [2 Hrs]

Histogram processing – [2 Hrs]

Basics of Spatial Filtering– [2 Hrs]

Smoothing and Sharpening Spatial filtering. [1 Hr]

4.2 IMAGE RESTORATION:

Image Restoration – [2 Hrs]

degradation model, [2 Hrs]

Noise models [1 Hr]

UNIT-V

IMAGE SEGMENTATION AND COMPRESSION **[11 Hrs]**

5.1 IMAGE SEGMENTATION:

Edge detection, [2 Hrs]

Region based segmentation – [2 Hrs]

Region growing – Region splitting and merging [2 Hrs]

5.2 IMAGE COMPRESSION:

Need for data compression, [1 Hr]

Huffman, Run Length Encoding, [2 Hrs]

Shift codes, Arithmetic coding, [1 Hr]

JPEG standard, MPEG [1 Hr]

Tests & Model Exam **[9 Hrs]**

TEXT BOOKS:

S.No	Title	Author	Publisher with Edition
1.	Signals, System and communication	B.P.Lathi	B.S Publication,2003
2.	Signals and Systems	A.V. Oppenheim, A.S. willsky and S.H. Nawab	PHI 2nd Edition

REFERENCE BOOKS:

S.No	Title	Author	Publisher with Edition
1.	Signals and Systems	Simon Haykin	van. Veen.Wiley, 2ndEdition
2.	Digital Image processing	RafelC.Gonzalez and Richard E woods	Pearson Inc 4th Edition –2018
3.	Fundamental of Digital Image processing	Anil K-Jain	Pearson Education, Inc – 2002

LEARNING WEBSITES:

1.https://www.robots.ox.ac.uk/~sjrob/Teaching/B4_SP/b4_sp.pdf

2.https://www.tutorialspoint.com/dip/index.htm

3. https://www.geeksforgeeks.org/digital-image-processing-basics/

4. https://www.slideshare.net/mathupuji/digital-image-processing-image-compression

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	-	**25 Marks**

CO-POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
D533.1	3	2	2	2	2	2	2	2	2	2
D533.2	3	2	2	2	2	2	2	2	2	2
D533.3	3	2	2	2	2	2	2	2	2	2
D533.4	3	2	2	2	2	2	2	2	2	2
D533.5	3	2	2	2	2	2	2	2	2	2
D533 Total	15	10	10	10	10	10	10	10	10	10
Correlation Level	3	2	2	2	2	2	2	5	5	2

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD540 ANALOG AND DIGITAL COMMUNICATION PRACTICAL

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester: 16 Weeks

Course	Instruction		Examination			
	Hrs/ Week	Hrs/ Semester	Marks			Duration
Analog and Digital Communication Practical	5	80	Internal Assessment	Autonomous Examination	Total	
			25	100*	100	3Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

DETAILED ALLOCATION OF MARKS

S.NO	DESCRIPTION	MARKS
1	CIRCUIT DIAGRAM / BLOCK DIAGRAM	25
2	CONNECTION	30
3	EXECUTION & HANDLING OF EQUIPMENT	20
4	OUTPUT /RESULT	10
5	VIVA–VOCE	5
6	MINI PROJECT	10
TOTAL		**100**

Mini Project Evaluation (10 marks)

Breakup Details

1	Project Description	05
2	Project Demo	05
	Total	**10**

COURSE DESCRIPTION

This laboratory is based on communication system based on analog and digital system. The Student will able to test various communication equipments including transmitter and receiver. This lab system enable students to apply many experiments and activities covers various topics in analog and digital communication system of different types which gain the various skill in day today life

EQUIPMENTS REQUIRED: (FOR A BATCH OF 30 STUDENTS)

S.No	Name of the Equipment	Range	Required Nos
1.	Dual trace CRO	100MHz	2
2.	ASK,FSK &PSK Modulation Kit	-	Each 1
3.	ASK,FSK &PSK Demodulation Kit	-	Each 1
4.	PCM Kit, TDM &Fiber optic demonstration kit	-	Each 1
5.	DTH	-	Each 1

OBJECTIVES:

On completion of the following experiments, the students must be able to

- know the concept of analog transmitter and receiver
- know the concept of digital (ASK/ FSK/PSK)
- Know about TDM
- Know the fiber optical link
- know the losses in optical fiber
- Test the performance of Manchester encoder and decoder
- know about DTH system
- Trace the PCM signal
- Develop the mini project

COURSE OUTCOMES

Course	ECD540 ANALOG AND DIGITAL COMMUNICATION PRACTICAL
After successful completion of this course, the students should be able to	
D540.1	Construct and test the sample and Hold Circuits, Amplitude Shift keying (ASK)Modulator and demodulator, Frequency Shift Keying(FSK) Modulator and Demodulator and Phase Shift Keying (PSK) Modulator and Demodulator.
D540.2	Test the performance of Time Division Multiplexer (TDM),Analog Transmitter and receiver and the horizontal and vertical deflection sensitivity of CRT.
D540.3	Test the performance of fiber optic analog link , digital link, Bending loss and propagation loss.
D540.4	Test the performance of Manchester encoder and decoder and voice link using optical fibre.
D540.5	Install and test a DTH system, trace the PCM Signal and develop mini project with report.

ECD540 ANALOG AND DIGITAL COMMUNICATION PRACTICAL

List of experiments to be conducted

1. Construct a sample and hold circuit, test and trace its waveforms.
2. Test the performance of ASK modulator and demodulator & draw its input and output waveform
3. Test the performance of FSK modulator and demodulator & draw its input and output waveform
4. Test the performance of PSK modulator and demodulator & draw its input and output waveform
5. Test the performance of Time Division Multiplexer and draw its input and output waveforms
6. Test the performance of analog transmitter and receiver and draw its input and output waveforms
7. Test the performance of a fiber optic analog link and draw its input and output waveforms
8. Test the performance of a fiber optic digital link and draw its input and output waveforms
9. Find the bending loss and propagation loss in fiber with two different fiber lengths
10. Test the performance of Manchester encoder and decoder using optical communication.
11. Test the performance of a voice link using optical fiber.
12. Test the Horizontal and Vertical deflection sensitivity of CRT.
13. Install a DTH system and test its performance.
14. Trace the output waveform of PCM signal.
15. Mini project

The mini project is activity based and it may be given to group of maximum of six students for hands on experience and to create scientific temper**.**

Continuous Internal Assessment

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:

a) Attendance (Award of marks same as theory courses)	:	05 Marks
b) Procedure/ observation and tabulation/ Other Practical related Work	:	05 Marks
c)Tests	:	10 Marks
d) Student Centered Learning (SCL) work sheet	:	05 Marks
Total		25 Marks

LEARNING WEBSITES

1. https://mrcet.com/downloads/ECE/ECE%20III-I.pdf
2. https://youtu.be/bBAdy40LArQ
3. https://youtu.be/SDA3tvGcB10
4. https://nevonprojects.com/project-ideas/electronics-ideas/

3CO- POs & PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
D540.1	3	3	3	3	3	3	3	3	3	3
D540.2	3	3	3	3	3	3	3	3	3	3
D540.3	3	3	3	3	3	3	3	3	3	3
D540.4	3	3	3	3	3	3	3	3	3	3
D540.5	3	3	3	3	3	3	3	3	3	3
D540 Total	15	15	15	15	15	15	15	15	15	15
Correlation Level	3	3	3	3	3	3	3	3	3	3

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

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ECD540 ANALOG AND DIGITAL COMMUNICATION PRACTICAL

MODEL QUESTION PAPER

S.No	Experiments	CO	PO
1	Construct a sample and hold circuit, test and trace its waveforms.	D540.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
2	Test the performance of ASK modulator and demodulator & draw its input and output waveform	D540.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
3	Test the performance of FSK modulator and demodulator & draw its input and output waveform	D540.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
4	Test the performance of PSK modulator and demodulator & draw its input and output waveform	D540.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
5	Test the performance of Time Division Multiplexer and draw its input and output waveforms	D540.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
6	Test the performance of analog transmitter and receiver and draw its input and output waveforms	D540.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
7	Test the performance of a fiber optic analog link and draw its input and output waveforms	D540.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
8	Test the performance of a fiber optic digital link and draw its input and output waveforms	D540.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
9	Find the bending loss and propagation loss in fiber with two different fiber lengths	D540.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
10	Test the performance of Manchester encoder and decoder using optical communication	D540.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
11	Test the performance of a voice link using optical fiber.	D540.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
12	Test the Horizontal and Vertical deflection sensitivity of CRT	D540.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
13	Install a DTH system and test its performance	D540.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
14	Trace the output waveform of PCM signal	D540.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
15	**Mini Project**	**D540.5**	**PO1,PO2,PO3,PO4, PO5,PO6,PO7**

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ECD550 MICROCONTROLLER PRACTICAL

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester: 15 Weeks

Course	Instruction		Examination			
Microcontroller Practical	Hrs. Week	Hrs Semester	Marks			Duration
			Internal Assessment	Autonomous Examination	Total	
	4	64	25	100*	100	3Hrs

***Examinations will be conducted for 100 marks will be reduced to 75 marks.**

DETAILED ALLOCATION OF MARKS

S.NO	DESCRIPTION	MARKS
1	ALGORITHM/FLOW CHART	20
2	PROGRAM	30
3	EXECUTION	30
4	RESULT	05
5	VIVA–VOCE	05
6	MINI PROJECT	10
TOTAL		**100**

Mini Project Evaluation (10 marks)

Breakup Details

1	Project Description	05
2	Project Demo	05
	Total	**10**

COURSE DESCRIPTION:

The introduction of this course will enable the students to have hands on experience in using 8051 trainer kit. The students are exposed to learn simple programs using assembly language. They can also get familiar with the C compiler platform. They also gain knowledge by using application specific interfacing boards.

EQUIPMENTS REQUIRED: (FOR A BATCH OF 30 STUDENTS)

S. No	Name of the Equipments	Required Nos
1.	8051 Microcontroller kit	14
2.	Digital I/O Interface board	2
3.	Seven segment LED display interface board	2
4.	8 bit DAC interface board	2
5.	Stepper motor control interface board	2
6.	DC motor control interface board	2
7.	RS 232 serial port cable	2
8.	LCD interface board	2
9.	Laptop / Desktop Computer	6

OBJECTIVES:

The students are able to

- Understand the use of instruction set by writing and executing simple ALP.
- Know the connection details between microcontroller and peripherals.
- Develop the mini projects.

COURSE OUTCOMES

Course	**ECD550 MICROCONTROLLER PRACTICAL**
After successful completion of this course, the students should be able to	
D550.1	Write and execute the assembly language program for addition, subtraction, multiplication and division of numbers.
D550.2	Write and verify the outputs of LEDS, DAC interface, LCD interface and digital I/O interface stepper motor and timer/counter.
D550.3	Write and convert ALP for converting numbers from BCD to hexadecimal, hexadecimal to BCD and finding smallest number.
D550.4	Write and perform serial communication between two 8051 microcontrollers, interface seven segment display and interface DC motor.
D550.5	Write a ALP for generating 10 KHz square wave and develop mini project with report.

ECD550 MICROCONTROLLER PRACTICAL

Part A

The following experiments should be written using 8051 assembly language program and should be executed in 8051 microcontroller kit.

1. 8 / 16 bit addition
2. 8 / 16 bit subtraction
3. 8 bit multiplication
4. 8 bit division
5. BCD to Hex code conversion
6. Hex to BCD code conversion
7. Smallest/Biggest number
8. Time delay routine (Demonstrate by Blinking LEDS).
9. Using Timer/counter of 8051.

Part B (Interfacing Application Boards)

The following experiments can be written using C compiler or 8051 assembly language and to be executed.

10. Interfacing Digital I/O board
11. Interfacing DAC
12. Interfacing Stepper motor
13. Interfacing Seven segment LED display or LCD
14. Sending data through the serial port between microcontroller kits
15. Interfacing DC motor using PWM.
16. Write assembly language programme to generate 10 KHz square wave.
17. Mini Project

The mini project is activity based and it may be given to group of maximum of six students for hands on experience and to create scientific temper.

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:

a) Attendance (Award of marks same as theory courses)	:	05 Marks
b) Procedure/ observation and tabulation/ Other Practical related Work	:	05 Marks
c)Tests	:	10 Marks
d) Student Centered Learning (SCL) work sheet	:	05 Marks

Total		25 Marks

LEARNING WEBSITES

1. https://www.elprocus.com/advanced-microcontroller-based-mini-projects-for-engineering-students
2. https://atria.edu/assets/ece/manuals/mc.pdf
3. https://www.electronicshub.org/microcontroller-based-mini-projects-ideas
4. https://nevonprojects.com/microcontroller-based-projects/

CO- POs & PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
D550.1	3	3	3	3	3	3	3	3	3	3
D550.2	3	3	3	3	3	3	3	3	3	3
D550.3	3	3	3	3	3	3	3	3	3	3
D550.4	3	3	3	3	3	3	3	3	3	3
D550.5	3	3	3	3	3	3	3	3	3	3
D550 Total	15	15	15	15	15	15	15	15	15	15
Correlation Level	3	3	3	3	3	3	3	3	3	3

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

ECD550 MICROCONTROLLER PRACTICAL

MODEL QUESTION PAPER

S.No	Experiments	CO	PO
1	Write an assembly language program for adding two 8 bit / 16 bit numbers and execute the same using 8051 trainer kit. Store the output result in memory. Input numbers can be given as immediate data or can be stored in the memory.	D550.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
2	Write a program to interface stepper motor with microcontroller 8051 and execute. Check the execution for varying the speed of the motor and also the forward/reverse rotation of the motor.	D550.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
3	Write a 8051 Assembly Language program to use Timer/ Counter of 8051 microcontroller to generate time delay and observe the output.	D550.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
4	Write a 8051 Assembly language program to generate 1 second time delay using Time delay routine and verify the output at LEDS.	D550.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
5	Write a program to interface DAC interface board with microcontroller and verify the analog output.	D550.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
6	Write a program to interface LCD interface board with microcontroller and observe the output at LCD.	D550.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
7	Write a program to interface Digital I /O board with microcontroller and verify all input and output operations.	D550.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
8	Write an assembly language program using 8051 to convert the given BCD number to hexadecimal number and store the result in memory. The input can be given as an immediate data or can be stored in the memory.	D550.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
9	Write an assembly language program using 8051 to convert the given hexadecimal number to BCD number and store the result in memory. The input can be given as an immediate data or can be stored in the memory.	D550.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
10	Write an assembly language program using 8051 to find the smallest number of the array of given numbers and store the result in the memory. The size of the array and the input numbers can be stored in the memory.	D550.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
11	Write an assembly language program using 8051 to perform 8 bit multiplication and store the result in the memory. The input numbers can be given as immediate data or can be stored in the memory.	D550.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7

12	Write an assembly language program for subtracting two 8 bit / 16 bit numbers and execute the same using 8051 trainer kit. Store the output result in memory. Input numbers can be given as immediate data or can be stored in the memory.	D550.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
13	Write an assembly language program using 8051 to perform 8 bit division and store the result in the memory. The input numbers can be given as immediate data or can be stored in the memory.	D550.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
14	Write a program to perform serial communication between two 8051 microcontroller kits and verify the output.	D550.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
15	Write a program to interface seven segment LED interface with microcontroller and verify the output at seven segment display.	D550.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
16	Write a program to interface a DC motor with microcontroller and verify the rotation of motor in both directions using PWM method.	D550.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
17	Write assembly language program to generate 10KHz square wave.	D550.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
18.	**Mini Project**	**D550.5**	**PO1,PO2,PO3,PO4, PO5,PO6,PO7**

ECD561 VERY LARGE SCALE INTEGRATION PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

No. of weeks per semester: 16 weeks

Course	Instruction		Examination			
			Marks			
	Hrs/Week	Hrs / Semester	Internal Assessment	Autonomous Examination	Total	Duration
Very Large Scale Integration Practical	5	80	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

DETAILED ALLOCATION OF MARKS

S.NO	DESCRIPTION	MARKS
1	ALGORITHM/FLOWCHART	30
2	PROGRAM	30
3	EXECUTING PROGRAM	20
4	OUTPUT /RESULT	05
5	VIVA–VOCE	05
6	MINI PROJECT	10
TOTAL		**100**

Mini Project Evaluation (10 marks)

Breakup Details

1	Project Description	05
2	Project Demo	05
	Total	**10**

COURSE DESCRIPTION :

VHDL is a versatile and powerful hardware description language which is useful for modeling digital systems at various levels of design abstraction. This language is mainly for describing the hardware. Execution of a VHDL program results in a simulation of the digital system allows us to validate the

design prior to fabrication of Digital Integrated circuit. This practical will enable the students to have hands on experience in using FPGA kit. The students are exposed to do programming in VHDL.

EQUIPMENTS REQUIRED: (FOR A BATCH OF 30 STUDENTS)

S.No	Name of the Equipments	Required Nos
1	FPGA KIT(at least 10 switches for input)	10
2	8 LEDs for output a 7 segment display	4
3	Debounced push switch	2
4	Clock input and external clock	10

OBJECTIVES:

The students will be able to

1. Understand the use of VHDL statements by writing program in VHDL.
2. Develop a VHDL code for any digital circuits.
3. Understand the concepts of digital circuits / logic function by simulating VHDL programs through XILINX software.
4. Understand the concepts of digital circuits by using FPGA kit.
5. To know the usage of input switches, output LEDs and seven segment display in FPGA kit.

COURSE OUTCOMES

Course	**ECD561 VERY LARGE SCALE INTEGRATION PRACTICAL**
After successful completion of this course, the students should be able to	
D561.1	Develop the VHDL codes for logic gates ,Combinational Circuit, Multiplexer/Demultiplexer, Half adder and Half subtractor, Full Adder And Full Subtractor.
D561.2	Develop the VHDL codes for single bit digital comparator, 8 to 1 Multiplexer/1 to 8 Demultiplexer and JK Flip flop
D561.3	Design and implement VHDL code for seven segment decoder, 7 segment display with counter ,8 to 3 encoder and 2 to 4 decoder.
D561.4	Design and implement VHDL code for blinking a LED and blinking array of LEDs and speller with array of LEDs.
D561.5	Develop a VHDL code for specified delayed output 1 second and 2 second by assuming clock frequency and develop mini project with report.

ECD561 VERY LARGE SCALE INTEGRATION PRACTICAL

NOTE: Behavioral or Structural model can be used for all experiments.

1.SIMULATION OF VHDL CODE FOR LOGIC GATES (AND GATE,ORGATE)

Develop code for logic gates. Simulate the code in the software.

2. SIMULATION OF VHDL CODE FOR COMBINATIONAL FUNCTION

Optimize a 4 variable combinational function (SOP), describe it in VHDL code and simulate it. Example: F=(0,1,4,5,8,9,12)in sop

3. SIMULATION OF VHDL CODE FOR HALF ADDER AND FULL ADDER

Develop code for half adder and full adder. Simulate the code in the software .

4. SIMULATION OF VHDL CODE FOR HALF SUBTRACTOR AND FULL SUBTRACTOR

Develop code for half subtractor and full subtractor. Simulate the code in the software.

5. SIMULATION OF VHDL CODE FOR SINGLE BIT DIGITAL COMPARATOR

Develop Boolean expression for A>B, A=B, A<B, write a VHDL code and simulate the code in the software.

6. VHDL IMPLEMENTATION OF 8 TO 1 MULTIPLEXER

Develop the code for a 8 to 1 multiplexer and implement it in FPGA kit in which switches are connected for select inputs and for data inputs, a LED is connected to the output.

7. VHDL CODE FOR JK FLIPFLOP (SIMULATION/IMPLEMENTATION)

Develop the code for JK flip flop and simulate using software or implement it in FPGA kit.

8. VHDL IMPLEMENTATION OF 1 TO 8 DEMULTIPLEXER

Develop the code for a 1 to 8 Demultiplexer and implement it in FPGA kit in which Switches are connected for select inputs and a data input, Eight LEDs are connected to the output of the circuit.

9. VHDL IMPLEMENTATION OF 7 SEGMENT DECODER – BOOLEAN EXPRESSION

Develop Boolean expression for4 input variables and 7output variables. Develop a seven segment decoder in VHDL for 7 equations. A seven segment display is connected to the output of the circuit. Four switches are connected to the input. The 4 bit input is decoded to 7 segment equivalent.

10. VHDL IMPLEMENTATION OF 7 SEGMENT DISPLAY – WITHCOUNTER

Design and develop a seven segment decoder in VHDL. Design and develop a 4 bit BCD counter, the output of the counter is given to seven segment decoder. A seven segment display is connected to the output of the decoder. The display shows 0,1,2..9 for every one second.

11. VHDL IMPLEMENTATION OF 8 TO 3 ENCODER

Develop code for 8 to 3 encoder. There will be 8 switches and 3 LEDs in the FPGA kit. The input given from switches and it is noted that any one of the switch is active. The binary equivalent for the corresponding input switch will be glowing in the LED as output.

12. VHDL IMPLEMENTATION OF 2 TO 4 DECODER

Develop code for 2 to 4 decoder and implement it in FPGA kit in which 2 Switches are connected for inputs , four LEDs for output.

13. VHDL IMPLEMENTATION FOR BLINKING A LED

Develop a VHDL Code for delay .Delay is adjusted in such a way that LED blinks for every 1 or 2seconds.

14. VHDL IMPLEMENTATION FOR BLINKING AN ARRAY OF LEDS

Design and develop a VHDL Code for 4 bit binary up counter. Four LEDs are connected at the output of the counter. The counter should up for every one seconds.

15. VHDL IMPLEMENTATION OF A SPELLER WITH AN ARRAY OF LEDS

Design and develop VHDL Code for a 5 bit Johnson ring counter 4 bit The LEDs are connected at the output of the counter. The speller should work for everyone seconds.

16. VHDL IMPLEMENTATION FOR MAKING A DELAYED OUTPUT

Develop a VHDL code for making a delayed output for 1 second or 2 seconds by assuming clock frequency provided in FPGA kit.

17. MINI PROJECT

The mini project is activity based and it may be given to group of maximum of six students for hands on experience and to create scientific temper.

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:

a) Attendance (Award of marks same as theory courses)	:	05 Marks
b) Procedure/ observation and tabulation/ Other Practical related Work	:	05 Marks
c)Tests	:	10 Marks
d) Student Centered Learning (SCL) work sheet	:	05 Marks

Total		25 Marks

LEARNING WEBSITES

1. https://www.studocu.com/in/document/chandigarh-university/computer-science-engneering/lab-manual-of-vls/11689201
2. https://www.skyfilabs.com/project-ideas/latest-projects-based-on-vlsi-design
3. http://grt.edu.in/ECEinnovate/LAB%20MANUAL/VLSI%20DESIGN%20LAB%20MANUAL.pdf

CO- POs & PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
D561.1	3	3	3	3	3	3	3	3	3	3
D561.2	3	3	3	3	3	3	3	3	3	3
D561.3	3	3	3	3	3	3	3	3	3	3
D561.4	3	3	3	3	3	3	3	3	3	3
D561.5	3	3	3	3	3	3	3	3	3	3
D561 Total	15	15	15	15	15	15	15	15	15	15
Correlation Level	3	3	3	3	3	3	3	3	3	3

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

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ECD561 VERY LARGE SCALE INTEGRATION PRACTICAL

MODEL QUESTION PAPER

S.No	Experiments	CO	PO
1	Write a VHDL code for logic gates (AND gate, OR gate) and simulate the code.	D561.1	PO1,PO2,PO3,PO4 ,PO5,PO6,PO7
2	Simplify the function f=(0,1,4,5,8,9,12). Write a VHDL code for the simplified function and simulate it	D561.1	PO1,PO2,PO3,PO4 ,PO5,PO6,PO7
3	Write a VHDL code for half adder and full adder and simulate the code	D561.1	PO1,PO2,PO3,PO4 ,PO5,PO6,PO7
4	Write a VHDL code for half subtractor and full subtractor and simulate the code	D561.1	PO1,PO2,PO3,PO4 ,PO5,PO6,PO7
5	Write a VHDL code for single bit digital comparator and simulate the code	D561.2	PO1,PO2,PO3,PO4 ,PO5,PO6,PO7
6	Write a VHDL code for 8 to 1 multiplexer and implement it in FPGA kit	D561.2	PO1,PO2,PO3,PO4 ,PO5,PO6,PO7
7	Write a VHDL code for JK flip flop and simulate using software or implement it in FPGA kit.	D561.2	PO1,PO2,PO3,PO4 ,PO5,PO6,PO7
8	Write aVHDLcodefor1 to 8 demultiplexer and implement it in FPGA kit.	D561.2	PO1,PO2,PO3,PO4 ,PO5,PO6,PO7
9	Write a VHDL code for 7 segment decoder – Boolean expression and implement it in FPGA kit.	D561.3	PO1,PO2,PO3,PO4 ,PO5,PO6,PO7
10	Write a VHDL code for 7 segment display - with counter and implement it in FPGA kit.	D561.3	PO1,PO2,PO3,PO4 ,PO5,PO6,PO7
11	Write a VHDL code for 8 to 3 encoder and implement it in FPGA kit.	D561.3	PO1,PO2,PO3,PO4 ,PO5,PO6,PO7
12	Write a VHDL code for 2 to 4 decoder and implement it in FPGA kit	D561.3	PO1,PO2,PO3,PO4 ,PO5,PO6,PO7
13	Write a VHDL code for blinking a LED and implement it in FPGA kit.	D561.4	PO1,PO2,PO3,PO4 ,PO5,PO6,PO7
14	Write a VHDL code for blinking an array of LEDs and implement it in FPGA kit.	D561.5	PO1,PO2,PO3,PO4 ,PO5,PO6,PO7
15	Write a VHDL code for speller with an array of LEDs and implement it in FPGA kit.	D561.4	PO1,PO2,PO3,PO4 ,PO5,PO6,PO7
16	Develop a VHDL code for making a delayed output for 1 second or 2 seconds by assuming clock frequency provided in FPGA kit.	D561.5	PO1,PO2,PO3,PO4 ,PO5,PO6,PO7
17	**Mini Project**	**D561.5**	**PO1,PO2,PO3,PO 4,PO5,PO6,PO7**

ECD562 CONSUMER ELECTRONICS PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

No. of weeks/ Semester : 16 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hours /week	Hours /semester	Internal Assessment	Autonomous Examination	Total	
Consumer Electronics Practical	5	80	25	100*	100	3 Hours

*** Examination will be conducted for 100 marks and it will be reduced to 75 marks.**

DETAILED ALLOCATION OF MARKS

S.NO	DESCRIPTION	MARKS
1	CIRCUIT DIAGRAM	25
2	PROCEDURE	30
3	EXECUTION &HANDLING OF EQUIPMENT	20
4	OUTPUT /RESULT	10
5	VIVA–VOCE	5
6	MINI PROJECT	10
	TOTAL	**100**

Mini Project Evaluation (10 marks)

Breakup Details

1	Project Description	05
2	Project Demo	05
	Total	**10**

COURSE DESCRIPTION:

The objective of teaching this course is to give students an in depth knowledge of various electronic audio and video devices and systems. Further this course will introduce the students with working principles, block diagram, main features of consumer electronics gadgets/goods/devices. This in-turn will develop in them capabilities of assembling, fault diagnosis and rectification in a systematic way.

LIST OF EQUIPMENTS: (FOR A BATCH OF 30 STUDENTS)

S.NO	Name of the Equipments	Quantity
1.	Digital Multimeter	10
2.	Microphone (Different types)	10
3.	Loud Speaker	10
4.	LED TV	2
5.	Dish Antenna	1
6.	Microwave Oven, Washing machine, A/C	2
7.	Digital Camera, Smart Phone/Tablet, Camcorder	2
8.	LCD/LED Projector.	2
9.	CCTV Cameras	5

OBJECTIVES:

On Completion of the following experiments the students must be able to

- Troubleshoot different types of Microphones and loudspeakers.
- Maintain and Troubleshoot of audio systems.
- Troubleshoot LED TV Receiver
- Know about installation and troubleshoot of CCTV and Dish antenna.
- Know about various sensors and their functionalities of washing machine.
- Know about installation and troubleshoot of A/C
- Maintain various consumer Electronics appliances.

COURSE OUTCOMES

Course	**ECD562 CONSUMER ELECTRONICS PRACTICAL**
After successful completion of this course, the students should be able to	
D562.1	Understand Public Address System, directional response of microphone and directional response of loudspeaker.
D562.2	Know the troubleshoot and fault identification CD/DVD player and LED TV, installation of Dish Antenna and CCTV System.
D562.3	Demonstrate Microwave oven, Automatic Washing Machine, Air conditioner and know the parameters in the smart phone , Tablet and digital camera settings.
D562.4	Build and test temperature control system , A/C motor control and verify functions of Camcorder.
D562.5	Install LCD /LED Projector and develop mini project with report.

ECD562 CONSUMER ELECTRONICS PRACTICAL

1. To study public address system and its components.
2. To plot the directional response of a Microphone.
3. To plot the directional response of a Loud Speaker.
4. Trouble shooting of CD/DVD Player.
5. To perform fault identification in LEDTV.
6. Installation of Dish Antenna for best reception.
7. Installation of CCTV system.
8. Demonstration of Microwave Oven.
9. Demonstration of Automatic Washing Machine and locate various sensors used in that washing machines.
10. To study the various parameters in the Smartphone and Tablet.
11. Explore digital cameras settings.
12. To build and test temperature control system.
13. To build and test circuit for A/C motor control.
14. Verify functions of Camcorder.
15. Installation of LCD/LED Projector and verify the functionalities.
16. Demonstration of Air conditioner and locate various components used in the Air conditioner
17. Mini Project

    The mini project is activity based and it may be given to group of maximum of six students for hands on experience and to create scientific temper.

Continuous Internal Assessment

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:

a) Attendance (Award of marks same as theory courses)	:	05 Marks
b) Procedure/ observation and tabulation/ Other Practical related Work	:	05 Marks
c)Tests	:	10 Marks
d) Student Centered Learning (SCL) work sheet	:	05 Marks

Total		25 Marks

LEARNING WEBSITES

1. https://www.sciencedirect.com/topics/engineering/consumer-electronics
2. https://www.techopedia.com/definition/757/consumer-electronics-ce
3. https://www.studocu.com/in/document/sir-pp-institute-of-science/bioquimica/consumer-electronics-lab-manual-exp-1/21667444

CO- POs & PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
D562.1	3	3	3	3	3	3	3	3	3	3
D562.2	3	3	3	3	3	3	3	3	3	3
D562.3	3	3	3	3	3	3	3	3	3	3
D562.4	3	3	3	3	3	3	3	3	3	3
D562.5	3	3	3	3	3	3	3	3	3	3
D562 Total	15	15	15	15	15	15	15	15	15	15
Correlation Level	3	3	3	3	3	3	3	3	3	3

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

ECD562 CONSUMER ELECTRONICS PRACTICAL

MODEL QUESTION PAPER

S.No	Experiments	CO	PO
1	To study public address system and its components.	D562.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
2	To plot the directional response of a Microphone.	D562.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
3	To plot the directional response of a Loud Speaker	D562.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
4	Trouble shooting of CD/DVD Player	D562.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
5	To perform fault identification in LED TV.	D562.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
6	Installation of Dish Antenna for best reception	D562.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
7	Installation of CCTV system	D562.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
8	Demonstration of Microwave Oven	D562.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
9	Demonstration of Automatic Washing Machine and locate various sensors used in that washing machines	D562.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
10	To study the various parameters in the Smartphone and Tablet	D562.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
11	Explore digital cameras settings.	D562.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
12	To build and test temperature control system	D562.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
13	To build and test circuit for A/C motor control	D562.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
14	Verify functions of Camcorder.	D562.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
15	Installation of LCD/LED Projector and verify the functionalities	D562.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
16	Demonstration of Air conditioner and locate various components used in the Air conditioner	D562.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
17	**Mini Project**	**D562.5**	PO1,PO2,PO3,PO4, PO5,PO6,PO7

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ECD563 SIGNAL AND IMAGE PROCESSING PRACTICAL

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 16 Weeks

Course	Instruction		Examination			
	Hrs/ Week	Hrs/ Semester	Marks			Duration
			Internal Assessment	Autonomous Examination	Total	
Signal and Image Processing Practical	5	80	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks**

DETAILED ALLOCATION OF MARKS

SL.NO	DESCRIPTION	MARKS
1	WRITING PROGRAM	40
2	EXECUTION OF PROGRAM	35
3	OUTPUT /RESULT	10
4	VIVA–VOCE	05
5	MINI PROJECT	10
	TOTAL	**100**

Mini Project Evaluation (10 marks)

Breakup Details

1	Project Description	05
2	Project Demo	05
	Total	**10**

COURSE DESCRIPTION

This laboratory makes the student to understand the basic concepts of signal and image processing. signal processing focuses on analyzing, modifying and synthesizing signals such as sound, images and scientific measurements. The need to extract information from images and interpret their contents has been one of the driving factors in the development of image processing and computer vision during the past decades. Image processing application cover a wide range of human activities such as Medical application, Industrial, Military, Consumer Electronics, Law Enforcement and security, the internet particularly the world wide web.

EQUIPMENTS REQUIRED: (FOR A BATCH OF 30 STUDENTS)

S.NO	Name of the Equipments	Range	Required Nos.
1.	Desk Top Computer	--	30
2.	Simulation Tool	MATLAB	1

OBJECTIVES :

On completion of the following experiments, the students must be able to

- know to generate discrete sequence signal.
- know about Fourier transform.
- know first order low pass filter and first order high pass filter.
- know about spatial domain.
- know about contrast stretching.
- know gray level slicing and bit plane slicing.
- know about masking.
- know frequency domain of ideal low pass filter and ideal high pass filter.
- Develop the mini projects

COURSE OUTCOMES

Course	**ECD563 SIGNAL AND IMAGE PROCESSING PRACTICAL**
After successful completion of this course, the students should be able to	
D563.1	Write MATLAB program to generate discrete sequence unit step, unit impulse,ramp and periodic sinusoidal signal,random sinusoidal signal and Fourier transform of square pulse.
D563.2	Write MATLAB program for finding magnitude and phase response of first order Low pass filter ,High pass filter, spatial domain for images.
D563.3	Write MATLAB program for power law transformation in spatial domain, contrast stretching and linear filter.
D563.4	Write MATLAB program gray level slicing and bit plane slicing, histogram equalization, and unsharp masking.
D563.5	Write MATLAB program for ideal LPF, ideal HPF ,Simulate the FIR filters and develop mini project with report.

ECD563 SIGNAL AND IMAGE PROCESSING PRACTICAL

List of experiments to be conducted

1. Write a MATLAB program to generate the discrete sequence unit step and unit impulse. Plot all sequences.
2. Write a MATLAB program to generate the discrete sequence ramp and periodic sinusoidal signal. plot all sequences.
3. Find the Fourier transform of a square pulse using MATLAB. Plot its amplitude and phase spectrum.
4. Write a MATLAB program to generate a random sinusoidal signal and plot four possible realizations of random signals.
5. Write a MATLAB program to find the magnitude and phase response of first order low pass filter. Plot the responses in logarithmic scale.
6. Write a MATLAB program to find the magnitude and phase response of first order high pass filter. Plot the responses in logarithmic scale.
7. Write a MATLAB program in spatial domain for image negatives and log transformation.
8. Obtain the power law transformation in spatial domain using MATLAB.
9. Write a MATLAB program for contrast stretching.
10. Write a MATLAB program in spatial domain for linear filter.
11. Write a MATLAB program for gray level slicing and bit plane slicing.
12. Write a MATLAB program for histogram equalization.
13. Write a MATLAB program for unsharp masking.
14. Obtain the frequency domain of ideal low pass filter using MATLAB.
15. Obtain the frequency domain of ideal high pass filter using MATLAB.
16. MATLAB simulation for FIR filters using windows technique (Rectangular, Hamming and Hanning).
17. Mini Project

    The mini project is activity based and it may be given to group of maximum of six students for hands on experience and to create scientific temper.

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:

a) Attendance (Award of marks same as theory courses)	:	05 Marks
b) Procedure/ observation and tabulation/ Other Practical related Work	:	05 Marks
c)Tests	:	10 Marks
d) Student Centered Learning (SCL) work sheet	:	05 Marks
Total		25 Marks

LEARNING WEBSITES

1. https://ssp-iiith.vlabs.ac.in/
2. https://www.vlab.co.in/broad-area-computer-science-and-engineering
3. https://vlead.vlabs.ac.in/#labs

COURSE OUTCOMES

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
D563.1	3	3	3	3	3	3	3	3	3	3
D563.2	3	3	3	3	3	3	3	3	3	3
D563.3	3	3	3	3	3	3	3	3	3	3
D563.4	3	3	3	3	3	3	3	3	3	3
D563.5	3	3	3	3	3	3	3	3	3	3
D563 Total	15	15	15	15	15	15	15	15	15	15
Correlation Level	3	3	3	3	3	3	3	3	3	3

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

ECD563 SIGNAL AND IMAGE PROCESSING PRACTICAL

MODEL QUESTION PAPER

Note: At least 5 experiments should be done using Soldering board / Bread board

S.No	Experiments	CO	PO
1	Write a MATLAB program to generate the discrete sequence unit step and unit impulse. Plot all sequences.	D563.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
2	Write a MATLAB program to generate the discrete sequence ramp and periodic sinusoidal signal. plot all sequences.	D563.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
3	Find the Fourier transform of a square pulse using MATLAB .Plot its amplitude and phase spectrum.	D563.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
4	Write a MATLAB program to generate a random sinusoidal signal and plot four possible realizations of random signals.	D563.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
5	Write a MATLAB program to find the magnitude and phase response of first order low pass filter. Plot the responses in logarithmic scale.	D563.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
6	Write a MATLAB program to find the magnitude and phase response of first order high pass filter. Plot the responses in logarithmic scale.	D563.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
7	Write a MATLAB program in spatial domain for image negatives and log transformation.	D563.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
8	Obtain the power law transformation in spatial domain using MATLAB .	D563.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
9	Write a MATLAB program for contrast stretching.	D563.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
10	Write a MATLAB program in spatial domain for linear filter.	D563.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
11	Write a MATLAB program for gray level slicing and bit plane slicing.	D563.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
12	Write a MATLAB program for histogram equalization.	D563.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7

13	Write a MATLAB program for unsharp masking.	D563.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
14	Obtain the frequency domain of ideal low pass filter using MATLAB.	D563.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
15	Obtain the frequency domain of ideal high pass filter using MATLAB.	D563.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
16	MATLAB simulation for FIR filters using windows technique (Rectangular, Hamming and Hanning)	D563.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
17	**Mini Project**	**D563.5**	**PO1,PO2,PO3,PO4, PO5,PO6,PO7**

ECD570 ENTREPRENEURSHIP AND START-UPS

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 16 weeks

Course	Instruction		Examination			
			Marks			
Entrepreneurship and start-ups	**Hrs/ Week**	**Hrs/ Semester**	**Internal Assessment**	**Autonomous Examination**	**Total**	**Duration**
	4	64	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

TOPICS AND ALLOCATION:

UNIT	TOPICS	NO. OF HOURS
I	Entrepreneurship – Introduction and Process	10
II	Business Idea and Banking	10
III	Start ups, E-cell and Success Stories	10
IV	Pricing and Cost Analysis	10
V	Business Plan Preparation	10
	Field Visit and preparation of case study report	14
TOTAL		**64**

COURSE DESCRIPTION:

Development of a diploma curriculum is a dynamic process responsive to the society and reflecting the needs and aspiration of its learners. Fast changing society deserves changes in educational curriculum particularly to establish relevance to emerging socio- economic environments; to ensure equity of opportunity and participation and finally promoting concern for excellence. In this context the course on entrepreneurship and start - ups aims at instilling and stimulating human urge for excellence by realizing individual potential for generating and putting to use the inputs, relevant to social prosperity and thereby ensure good means of living for every individual, provides jobs and develop Indian economy.

OBJECTIVES:

At the end of the study of 5th semester the students will be able to

- Excite the students about entrepreneurship.
- Acquiring Entrepreneurial spirit and resourcefulness.
- Understanding the concept and process of entrepreneurship.
- Acquiring entrepreneurial quality, competency and motivation.
- Learning the process and skills of creation and management of entrepreneurial venture
- Familiarization with various uses of human resource for earning dignified means of living.
- Know its contribution in and role in the growth and development of individual and the nation.
- Understand the formation of E-cell.
- Survey and analyze the market to understand customer needs.
- Understand the importance of generation of ideas and product selection.
- Learn the preparation of project feasibility report.
- Understand the importance of sales and turnover.
- Familiarization of various financial and non financial schemes.
- Aware the concept of incubation and start ups.

COURSE OUTCOMES

Course	**ECD570 ENTREPRENEURSHIP AND START-UPS**
After successful completion of this course, the students should be able to	
D570.1	Understand the concept and process of Entrepreneurship.
D570.2	Familiarize about business idea and banking.
D570.3	Understand the formation of E-Cell, start-ups and success stories.
D570.4	Aware about pricing and cost analysis
D570.5	Learn about the business plan preparation

ECD570 ENTREPRENEURSHIP AND START-UPS

UNIT I

ENTREPRENEURSHIP – INTRODUCTION AND PROCESS **[10 Hrs]**

Concept, Functions and Importance
Myths about Entrepreneurship
Pros and Cons of Entrepreneurship
Process of Entrepreneurship
Benefits of Entrepreneur
Competencies and characteristics
Ethical Entrepreneurship
Entrepreneurial Values and Attitudes
Motivation
Creativity
Innovation
Entrepreneurs - as problem solvers
Mindset of an employee and an entrepreneur Business Failure – causes and remedies
Role of Networking in entrepreneurship

UNIT II

BUSINESS IDEA AND BANKING **[10 Hrs]**

Types of Business: Manufacturing, Trading and Services
Stakeholders: Sellers, Vendors and Consumers
E-Commerce Business Models
Types of Resources-Human, Capital and Entrepreneurial tools
Goals of Business and Goal Setting
Patent, copyright and intellectual Property Rights
Negotiations- Importance and methods
Customer Relations and Vendor Management
Size and Capital based classification of business enterprises
Role of Financial Institutions
Role of Government Policy
Entrepreneurial support systems
Incentive schemes for State Government
Incentive Schemes for Central Government

UNIT III

START UPS, E-CELL AND SUCCESS STORIES **[10 Hrs]**

Concept of Incubation centres

Activities of DIC, financial institutions and other relevance institutions

Success stories of Indian and global business legends

Field Visit to MSMEs

Various sources of Information

Learn to earn

Startup and its stages

Role of Technology-E-commerce and Social Media

Role of E-Cell

E-Cell to Entrepreneurship

UNIT IV

PRICING AND COST ANALYSIS **[10 Hrs]**

Calculation of Unit of Sale, Unit Price and Unit Cost

Types of Costs - Variable and Fixed, Operational Costs

Break Even Analysis

Understand the meaning and concept of the term Cash Inflow and Cash Outflow

Prepare a Cash Flow Projection

Pricing and Factors affecting pricing

Understand the importance and preparation of Income Statement

Launch Strategies after pricing and proof of concept

Branding-Business name, logo, tag line

Promotion strategy

UNIT V

BUSINESS PLAN PREPARATION **[10 Hrs]**

Generation of Ideas

Business Ideas vs. Business Opportunities

Selecting the Right Opportunity

Product selection

New product development and analysis

Feasibility Study Report – Technical analysis, financial analysis and commercial analysis

Market Research - Concept, Importance and Process

Marketing and Sales strategy

Digital marketing

Social Entrepreneurship

Risk Taking-Concept

Types of business risks

Field Visit and preparation of case study report **[14 Hrs]**

TEXT BOOKS:

S.NO	TITLE	AUTHOR	PUBLISHER WITH EDITION
1.	Fundamentals of Entrepreneurship	Dr. G.K. Varshney	Sahitya Bhawan Publications, Agra -282002
2.	Business Regulatory Framework	Dr. G.K. Varshney	Sahitya Bhawan Publications, Agra - 282002

REFERENCE BOOKS:

S.NO	TITLE	AUTHOR	PUBLISHER WITH EDITION
1.	Entrepreneurship	Robert D. Hisrich, Michael P. Peters, Dean A. Shepherd	McGraw Hill (India) Private Limited, Noida - 201301
2.	Essentials of Entrepreneurship and small business management	M.Scarborough, R.Cornwell	Pearson Education India, Noida -201301
3.	Entrepreneurship Development and Small Business Enterprises	Charantimath Poornima M	Pearson Education, Noida -201301
4.	Innovation Management and New Product Development	Trott	Pearson Education, Noida -201301
5.	A Textbook of Cost and Management Accounting	M N Arora	Vikas Publishing House Pvt. Ltd., NewDelhi-110044
6.	Financial Management	Prasanna Chandra	Tata McGraw Hill education private limited, New Delhi
7.	Indian Banking System	I.V.Trivedi, Renu Jatana	RBSA Publishers, Rajasthan
8.	HOW TO START A BUSINESS IN INDIA	Simon Daniel	BUUKS, Chennai - 600018
9.	The Business Plan Write-Up Simplified	Ramani Sarada	A practitioners guide to writing the business plan, Notion press media Pvt.Ltd.,Chennai-600095

LEARNING WEBSITES:

1. https://www.startupindia.gov.in/
2. https://www.startupcommons.org/what-is-a-startup.html
3. https://www.forbes.com/sites/allbusiness/2018/07/15/35-step-guide-entrepreneurs-starting-a-business/
4. https://www.entrepreneur.com/topic/startups
5. https://www.investopedia.com/terms/s/startup.asp

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks
	Total	**-**	**25 Marks**

Note: Two assignments should be submitted. The same must be evaluated and converted to 5marks

Guidelines for assignment:

First assignment – Unit I

Second assignment – Unit II

Guidelines for Seminar presentation – Unit III

Each assignment should have five three marks questions and two five marks questions.

AUTONOMOUS EXAMINATION

Note

1. The students should be taught all units and proper exposure and filed visit also arranged. All the portions should be completed before examinations

2. The students should maintain theory assignment and seminar presentation. The assignment and seminar presentation should be submitted during the Autonomous Practical Examinations.

3. The question paper consists of theory and practical portions .All students should write the answers for theory questions (45 marks) and practical portions (55 marks) should be completed for Autonomous examinations

4. All exercises should be given in the question paper and students are allowed to select by lot. If required the dimension for the exercise may be varied for every batch. No fixed time allotted for each portion and students have the liberty to do the examinations for 3Hrs.

5. For Written Examination: theory question and answer:45 Marks

Ten questions will be asked for 3 marks each. Five questions from each unit 1&2 (10*3=30)

Three questions will be asked for 5 marks each. One questions from each unit 1,2&3 (3*5=15)

6. For Practical Examination: The business plan/Feasibility report or Report on Unit 4&5 should be submitted during the Autonomous practical examinations. The same have to be evaluated for the report submission(40 marks)

DETAILED ALLOCATION OF MARKS

S.NO	DESCRIPTION	MARKS
PART-A	Written Examination- Theory Question and answer (10 questions x 3marks:30 marks) & (3 questions x 5 marks:15 marks)	45
PART B	Practical examination – submission on business plan/ feasibility report or report on unit 4&5	40
PART C	Viva voce	15
	Total	**100**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
D570.1	3	3	2	2	2	2	2	3	2	2
D570.2	3	3	2	2	2	2	2	3	2	2
D570.3	3	3	2	2	2	2	2	3	2	2
D570.4	3	3	2	2	2	2	2	3	2	2
D570.5	3	3	2	2	2	2	2	3	2	2
D570Total	15	15	10	10	10	10	10	15	10	10
Correlation Level	3	3	2	2	2	2	2	3	2	2

Correlation level 1- Slight (low)
Correlation level 2- Moderate (Medium)
Correlation level 3- Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD570 ENTREPRENEURSHIP AND START-UPS

PART-A

MODEL QUESTION PAPER

TIME: 3 Hrs **MARKS: 45**

PART-I (10 X 3= 30 Marks)					
Note: Answer all questions. All questions carry equal marks					
S.No	**Questions**	**UNIT**	**Bloom's Level**	**CO**	**PO**
1	Define entrepreneurship.	I	R	D570.1	POI,PO2,PO3
2	State the process of entrepreneurship.	I	R	D570.1	POI,PO2,PO3
3	What are the benefits of being an entrepreneur?	I	R	D570.1	POI,PO2,PO3
4	How do entrepreneurs act as problem solvers?	I	U	D570.1	POI,PO2,PO3
5	Outline the role of networking in entrepreneurship.	I	U	D570.1	POI,PO2,PO3
6	List the various types of business.	II	R	D570.2	POI,PO2,PO3
7	Outline the business model.	II	U	D570.2	POI,PO2,PO3
8	Suggest the various goals of business.	II	U	D570.2	POI,PO2,PO3
9	How selection of human resources is carried out?	II	U	D570.2	POI,PO2,PO3
10	Specify the role of government policy on entrepreneurship.	II	U	D570.2	POI,PO2,PO3

PART-II (3 X 5 = 15Marks)					
Note: Answer all questions. All questions carry equal marks					
S.No	**Questions**	**UNIT**	**Bloom's Level**	**CO**	**PO**
11	Describe the importance of innovation on entrepreneurship.	I	An	D570.1	POI,PO2,PO3
12	Enumerate the various incentive schemes for the central government.	II	U	D570.2	POI,PO2,PO3
13	How technology will play a major role in E-commerce?	III	An	D570.3	POI,PO2,PO3

QUESTION PAPER SETTING

The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as Presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD510 ANALOG AND DIGITAL COMMUNICATION SYSTEMS

MODEL QUESTION PAPER

Time: 3 Hrs **Max. Marks: 100**

PART-A (10 X 3 = 30Marks)					
Note: Answer all questions. All questions carry equal marks.					
S.No	**Questions**	**UNIT**	**Bloom's Level**	**CO**	**PO**
1	State the factors governing maximum range of RADAR.	I	U	D510.1	PO1,PO2,PO3
2	What is Telephone system?	I	R	D510.1	PO1,PO2,PO3
3	Define odd parity and even parity.	II	U	D510.2	PO1,PO2,PO3
4	State the different modulation techniques used in digital communication.	II	U	D510.2	PO1,PO2,PO3
5	Mention the advantages of fiber optic communication.	III	U	D510.3	PO1,PO2,PO3
6	Differentiate single mode and multimode fiber.	III	U	D510.3	PO1,PO2,PO3
7	Draw the block diagram of Satellite transponder.	IV	U	D510.4	PO1,PO2,PO3
8	List the different types of Satellite orbit.	IV	U	D510.4	PO1,PO2,PO3
9	What is adjacent channel interference?	V	R	D510.5	PO1,PO2,PO3
10	Explain about development of wireless networks 3G,4G and 5G.	V	U	D510.5	PO1,PO2,PO3

	PART-B (5 X 14 = 70 Marks)					
	Note: Answer all questions choosing A or B in each question. All questions carry equal marks					
S.No	**Questions**	**Marks**	**UNIT**	**Bloom's Level**	**CO**	**PO**
11	(A) (i) Draw the block diagram of basic pulsed RADAR system and explain.	07	I	U	D510.1	PO1,PO2,PO3
	(ii) Give the applications of RADAR.	07	I	U	D510.1	PO1,PO2,PO3
	(OR)					
	(B) (i) Describe the ISDN architecture with a block diagram.	07	I	U	D510.1	PO1,PO2,PO3

	(ii) Explain Instrument Landing system.	07	1	U	D510.1	PO1,PO2,PO3
12	(A) (i) Explain any three characteristics of data transmission circuits.	07	II	U	D510.2	PO1,PO2,PO3
	(ii) Explain ASCII code	07	II	U	D510.2	PO1,PO2,PO3
	(OR)					
	(B) (i) Explain Error detection code	07	II	U	D510.2	PO1,PO2,PO3
	(ii) Explain Hamming code.	07	II	U	D510.2	PO1,PO2,PO3
13	(A).(i) Explain LASER diode operation with neat diagram.	07	III	U	D510.3	PO1,PO2,PO3
	(ii) Explain about Absorption losses in optical fiber.	07	III	U	D510.3	PO1,PO2,PO3
	(OR)					
	(B) (i) Explain any two applications of optical fiber with necessary diagrams.	07	III	U	D510.3	PO1,PO2,PO3
	(ii) Draw the block diagram of optical receiver and explain its operation.	07	III	U	D510.3	PO1,PO2,PO3
14	(A) (i) Explain with necessary block diagram of transmit and receive earth station.	07	IV	U	D510.4	PO1,PO2,PO3
	(ii) Explain Earth eclipse of satellite.	07	IV	U	D510.4	PO1,PO2,PO3
	(OR)					
	(B) (i) Explain with block diagram of microwave transmitter and receiver.	07	IV	U	D510.4	PO1,PO2,PO3
	(ii) Explain Parabolic reflector antenna.	07	IV	U	D510.4	PO1,PO2,PO3
15	(A) (i) What is roaming?	07	V	U	D510.5	PO1,PO2,PO3
	(ii) Explain how hand-off takes place with neat diagram in four steps.	07	V	U	D510.5	PO1,PO2,PO3
	(OR)					
	(B) (i) Explain GSM architecture with neat diagram.	07	V	U	D510.5	PO1,PO2,PO3
	(ii) Explain Co-channel interference.	07	V	U	D510.5	PO1,PO2,PO3

QUESTION PAPER SETTING

The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as Presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD520 MICROCONTROLLER AND ITS APPLICATIONS

MODEL QUESTION PAPER

Time: 3 Hrs **Max.Marks:100**

PART-A (10 X 3 = 30Marks)					
Note: Answer all questions. All questions carry equal marks.					
S.No	**Questions**	**UNIT**	**Bloom's Level**	**CO**	**PO**
1	Write the comparison between microprocessor and microcontroller.	I	U	D520.1	PO1,PO2,PO3
2	Explain RESET.	I	U	D520.1	PO1,PO2,PO3
3	Give the classification of instruction set of 8051.	II	R	D520.2	PO1,PO2,PO3
4	List the addressing modes of 8051.	II	R	D520.2	PO1,PO2,PO3
5	Draw the bit configuration of TMOD register.	III	R	D520.3	PO1,PO2,PO3
6	Write down the interrupts of 8051.	III	U	D520.3	PO1,PO2,PO3
7	Define Interfacing.	IV	R	D520.4	PO1,PO2,PO3
8	How to interface relay with 8051?	IV	R	D520.4	PO1,PO2,PO3
9	Write down the features of Arduino.	V	R	D520.5	PO1,PO2,PO3
10	Explain about IoT applications.	V	U	D520.5	PO1,PO2,PO3

PART-B (5 X 14 = 70 Marks)						
Note: Answer all questions choosing A or B in each question. All questions carry equal marks						
S.No	**Questions**	**Marks**	**UNIT**	**Bloom's Level**	**CO**	**PO**
11	A. (i). Draw the Architecture diagram of 8051 Microcontroller.	07	I	U	D520.1	PO1,PO2,PO3
	(ii). Draw the pin configuration of 8051 and Explain in brief about each pin.	07	I	U	D520.1	PO1,PO2,PO3
	(OR)					
	B. (i). Explain the memory organization of 8051.	07	I	U	D520.1	PO1,PO2,PO3
	(ii). Explain about SFRs in brief.	07	1	U	D520.1	PO1,PO2,PO3

12	A. (i). Explain data transfer instructions of 8051with examples.	07	II	U	D520.2	PO1,PO2,PO3
	(ii). Write a 8051 Assembly language program for 8 bit multiplication.	07	II	U	D520.2	PO1,PO2,PO3,PO4
	(OR)					
	B. (i). List the addressing modes of 8051and explain any two modes in detail.	07	II	U	D520.2	PO1,PO2,PO3
	(ii) Write a 8051 Assembly language program for 16 bit addition.	07	II	U	D520.2	PO1,PO2,PO3,PO4
13	A. (i). Explain the modes of timer of 8051 with diagram.	07	III	U	D520.3	PO1,PO2,PO3
	(ii). Explain about RS232 standard in detail.	07	III	U	D520.3	PO1,PO2,PO3
	(OR)					
	B.(i). Explain the steps to program 8051 to transfer and receive data serially.	07	III	U	D520.3	PO1,PO2,PO3,PO4
	(ii). Explain about 8051 interrupts and priority in detail.	07	III	U	D520.3	PO1,PO2,PO3
14	A.(i) Draw the block diagram of 8255 and explain the function in detail.	07	IV	U	D520.4	PO1,PO2,PO3
	(ii) Draw the interfacing of 8255 with microcontroller and explain.	07	IV	U	D520.4	PO1,PO2,PO3
	(OR)					
	B.(i). Explain the interfacing of seven segment LED display with 8051 microcontroller with diagram	07	IV	U	D520.4	PO1,PO2,PO3
	(ii). Explain the interfacing of DAC with 8051 microcontroller and explain.	07	IV	U	D520.4	PO1,PO2,PO3

15	A.(i). Draw the block diagram of PIC microcontroller and explain.	07	V	U	D520.5	PO1,PO2,PO3
	(ii). Draw the block diagram of Arduino and explain.	07	V	U	D520.5	PO1,PO2,PO3
	(OR)					
	B. (i). Draw the block diagram of home automation using IoT and explain.	07	V	U	D520.5	PO1,PO2,PO3,PO4,PO5
	(ii). Draw the block diagram of Raspberry Pi and explain.	07	V	U	D520.5	PO1,PO2,PO3,PO4,PO5

QUESTION PAPER SETTING

The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as Presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD531 VERY LARGE SCALE INTEGRATION

MODEL QUESTION PAPER

TIME: 3 Hrs **Marks: 100**

PART-A (10 X 3 = 30Marks)					
Note: Answer any the questions. All questions carry equal marks.					
S.No	**Questions**	**UNIT**	**Bloom's Level**	**CO**	**PO**
1	Draw the circuit for NAND gate using NMOS.	I	U	D531.1	PO1,PO2
2	Draw the circuit for NOR gate using NMOS.	I	U	D531.1	PO1,PO2
3	What are the different types of modeling?.	II	R	D531.2	PO1,PO2
4	Write the VHDL code for AND gate.	II	An	D531.2	PO1,PO2,PO3
5	Write the VHDL code for Half adder.	III	An	D531.3	PO1,PO2,PO3
6	Differentiate behavioral and structural model.	III	An	D531.3	PO1,PO2,PO3
7	Write the VHDL code for D flipflop.	IV	An	D531.4	PO1,PO2,PO3
8	What is the difference between Ring counter and Johnson counter?	IV	R	D531.4	PO1,PO2,PO3
9	Compare PROM, PAL and PLA.	V	R	D531.5	PO1,PO2
10	Write short notes on ASIC.	V	R	D531.5	PO1,PO2

	PART-B (5 X 14 = 70 Marks)					
	Note: Answer all questions choosing A or B in each question. All questions carry equal marks.					
S.No	**Questions**	**Marks**	**UNIT**	**Bloom's Level**	**CO**	**PO**
11	A.(i). Implement the following functions a) Y=AB+CD b) Y= (A+B).(C+D) using CMOS.	07	I	An	D531.1	PO1,PO2,PO3,PO4
	(ii). Draw the circuit for AND, OR, NOT gate using NMOS and explain.	07	I	An	D531.1	PO1,PO2,PO3,PO4
	(OR)					
	B. (i). Draw the circuit for NAND, NOR, AND, OR gate using CMOS and explain.	07	I	An	D531.1	PO1,PO2,PO3,PO4

	(ii). Explain the steps involved in VLSI design process.	07	1	An	D531.1	PO1,PO2,PO3,PO4
12	A. (i). Write a VHDL program for logic gates OR gate, NOT gate.	07	II	An	D531.2	PO1,PO2,PO3,PO4
	(ii). Explain if statement, if else statement with example.	07	II	An	D531.2	PO1,PO2,PO3,PO4
	(OR)					
	B. (i). Write a VHDL program for logic gates NAND gate and NOR gate	07	II	An	D531.2	PO1,PO2,PO3,PO4
	(ii) Explain if ,elseif, else statement, case statement with example.	07	II	U	D531.2	PO1,PO2,PO3,PO4
13	A. (i). Write a VHDL program for 4 X 1 Multiplexer.	07	III	An	D531.3	PO1,PO2,PO3,PO4
	(ii). Write a VHDL program for 2 X 4 decoder.	07	III	An	D531.3	PO1,PO2,PO3,PO4
	(OR)					
	B.(i). Write a VHDL program for 1X 4 De Multiplexer.	07	III	An	D531.3	PO1,PO2,PO3,PO4
	(ii). Write a VHDL program for 4 X 2encoder.	07	III	An	D531.3	PO1,PO2,PO3,PO4
14	A.(i) Write a VHDL program for JK flip flop.	07	IV	An	D531.4	PO1,PO2,PO3,PO4
	(ii) Write a VHDL program for D flip flop.	07	IV	An	D531.4	PO1,PO2,PO3,PO4
	(OR)					
	B.(i). Write a VHDL program for Johnson counter.	07	IV	An	D531.4	PO1,PO2,PO3,PO4
	(ii).Write a VHDL program for Decade counter.	07	IV	An	D531.4	PO1,PO2,PO3,PO4
15	A.(i). Explain PLA with example.	07	V	U	D531.5	PO1,PO2,PO3,PO4
	(ii). Explain PAL with example.	07	V	U	D531.5	PO1,PO2,PO3,PO4
	(OR)					
	B. (i). Explain the architecture of FPGA	07	V	U	D531.5	PO1,PO2,PO3
	(ii). Explain design flow of ASIC	07	V	U	D531.5	PO1,PO2,PO3,PO4

QUESTION PAPER SETTING

The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as Presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD532 CONSUMER ELECTRONICS

MODEL QUESTION PAPER

TIME: 3 Hrs **MARKS: 100**

PART-A (10 X 3 = 30Marks)					
Note: Answer all questions. All questions carry equal marks					
S.No	**Questions**	**UNIT**	**Bloom's Level**	**CO**	**PO**
1	What are the limitations of crystal microphones?	I	U	D532.1	PO1,PO2
2	Discuss the difference between a microphone and a loudspeaker.	I	U	D532.1	PO1,PO2
3	Mention the various types of sound reproducing systems.	II	U	D532.2	PO1,PO2
4	Draw the block diagram of Home theater system.	II	R	D532.2	PO1,PO2
5	What are the advantages and disadvantages of PAL?	III	R	D532.3	PO1,PO2
6	What are the advantages and disadvantages of SECAM?	III	R	D532.3	PO1,PO2
7	List out the differences of LCD and LED TV.	IV	U	D532.4	PO1,PO2
8	Discuss the differences of SD and HDTV.	IV	U	D532.4	PO1,PO2
9	Write short note on fuzzy logic.	V	R	D532.5	PO1,PO2
10	State the pixel information of digital camera.	V	U	D532.5	PO1,PO2

PART-B (5 X 14 = 70 Marks)						
Note: Answer all questions choosing A or B in each question. All questions carry equal marks						
S.No	**Questions**	**Marks**	**UNIT**	**Bloom's Level**	**CO**	**PO**
11	A.(i). Explain the working of Carbon microphone with neat sketch.	07	I	U	D532.1	PO1,PO2,PO3, PO5
	(ii). Explain any one optical recording system with neat sketch.	07	I	U	D532.1	PO1,PO2,PO3, PO5
	(OR)					
	B. (i). Explain the working of Horn loudspeaker with neat sketch.	07	I	U	D532.1	PO1,PO2,PO3, PO5
	(ii). Explain the working of Magnetic recording with neat sketch.	07	1	U	D532.1	PO1,PO2,PO3, PO5
12	A. (i). Explain the working of Home theater system with suitable diagram.	07	II	U	D532.2	PO1,PO2,PO3, PO5
	(ii). Explain the working of digital sound recording of CD.	07	II	U	D532.2	PO1,PO2,PO3, PO5
	(OR)					
	B. (i). Explain the working of HI-Fi system with suitable diagram.	07	II	U	D532.2	PO1,PO2,PO3, PO5
	(ii) Explain the audio format MP3.	07	II	U	D532.2	PO1,PO2,PO3, PO5
13	A. (i). Explain the concept of luminance in color TV.	07	III	U	D532.3	PO1,PO2,PO3, PO5
	(ii). Explain the working of NTSC Color TV encoder with neat sketch.	07	III	U	D532.3	PO1,PO2,PO3, PO5
	(OR)					
	B.(i). Explain the concepts of additive and subtracting mixing of colours.	07	III	U	D532.3	PO1,PO2,PO3, PO5
	(ii). Explain construction and working principles of Trinitron.	07	III	U	D532.3	PO1,PO2,PO3, PO5
14	A.(i) Explain in detail about DTH	07	IV	U	D532.4	PO1,PO2,PO3,

	system with necessary diagram.					PO5
	(ii) Draw and Explain LCD TV with neat sketch.	07	IV	U	D532.4	PO1,PO2,PO3, PO5
	(OR)					
	B.(i). Explain in detail about video on demand.	07	IV	U	D532.4	PO1,PO2,PO3, PO5
	(ii).Explain the concepts of LED TV with neat block diagram.	07	IV	U	D532.4	PO1,PO2,PO3, PO5
15	A.(i).Explain the working of Microwave Oven with necessary diagram.	07	V	U	D532.5	PO1,PO2,PO3, PO5
	(ii).Explain the working of digital camera with neat sketch.	07	V	U	D532.5	PO1,PO2,PO3, PO5
	(OR)					
	B. (i).) Explain the working of Photostat Machine with neat sketch.	07	V	U	D532.5	PO1,PO2,PO3,PO5
	(ii). Explain the working of washing machine with its wiring diagram.	07	V	U	D532.5	PO1,PO2,PO3,PO5

QUESTION PAPER SETTING

The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as Presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD533 BASICS OF DIGITAL SIGNAL AND IMAGE PROCESSING

MODEL QUESTION PAPER

TIME: 3 Hrs **MARKS: 100**

PART-A (10 X 3 = 30Marks)					
Note: Answer all questions. All questions carry equal marks					
S.No	**Questions**	**UNIT**	**Bloom's Level**	**CO**	**PO**
1	Distinguish between periodic and Aperiodic signals.	I	U	D533.1	PO1,PO2
2	Define discrete time unit step and unit impulse function.	I	R	D533.1	PO1,PO2
3	Find the Laplace transform of an unit step function.	II	U	D533.2	PO1,PO2
4	What is the relationship between fourier transform and Laplace transform?	II	R	D533.2	PO1,PO2
5	What is digital image processing?	III	R	D533.3	PO1,PO2
6	What is dynamic Range?	III	R	D533.3	PO1,PO2
7	Explain the two categories of Image enhancement.	IV	U	D533.4	PO1,PO2
8	What is meant by Image restoration?	IV	R	D533.4	PO1,PO2
9	Write the application of Segmentations.	V	R	D533.5	PO1,PO2
10	What is different compression Methods?	V	U	D533.5	PO1,PO2

	PART-B (5 X 14 = 70 Marks)					
	Note: Answer all questions choosing A or B in each question. All questions carry equal marks					
S.No	**Questions**	**Marks**	**UNIT**	**Bloom's Level**	**CO**	**PO**
11	A.(i). Given Y(n) = nx(n) Determine whether the system is causal, linear,Time invariant and stable.	07	I	U	D533.1	PO1,PO2,PO3

	(ii) Describe the classification of systems.	07	I	U	D533.1	PO1,PO2,PO3
	(OR)					
	B. (i) Explain briefly about Continuous time (CT) and discrete time (DT) signals	07	I	U	D533.1	PO1,PO2,PO3
	(ii). Distinguish between random and deterministic signals.	07	1	U	D533.1	PO1,PO2,PO3
12	A. (i).Find the Trigonometric fourier series representation of aperiodic signal x(t)=t for the interval of t=-1 to t=1.	07	II	An	D533.2	PO1,PO2,PO3
	(ii). State and prove the parseval's theorem for fourier transform.	07	II	U	D533.2	PO1,PO2,PO3
	(OR)					
	B. (i). Obtain the Laplace transforms for the following (a) x(t)=t u(t) (b) x(t)= cosbt u(t).	07	II	An	D533.2	PO1,PO2,PO3
	(ii) Explain any two properties of Laplace Transform.	07	II	U	D533.2	PO1,PO2,PO3
13	A. (i). Explain the steps involved in digital Image processing.	07	III	U	D533.3	PO1,PO2,PO3
	(ii). Explain the image formation in the eye with brightness adaptation and discrimination.	07	III	U	D533.3	PO1,PO2,PO3
	(OR)					
	B.(i). Explain Basic concept of	07	III	U	D533.3	PO1,PO2,PO3

	Sampling and Quantization.					
	(ii). Explain the basic relationship between pixels.	07	III	U	D533.3	PO1,PO2,PO3
14	A.(i) Explain the types of Gray level transformation used for Image enhancement.	07	IV	U	D533.4	PO1,PO2,PO3
	(ii) Explain spatial filtering in image enhancement.	07	IV	U	D533.4	PO1,PO2,PO3
	(OR)					
	B.(i). Explain image restoration process in details.	07	IV	U	D533.4	PO1,PO2,PO3
	(ii). Explain Noise model.	07	IV	U	D533.4	PO1,PO2,PO3
15	A.(i). what is Image segmentation? explain in detail.	07	V	U	D533.5	PO1,PO2,PO3
	(ii). Explain Edge detection.	07	V	U	D533.5	PO1,PO2,PO3
	(OR)					
	B. (i). Explain about image compression model.	07	V	U	D533.5	PO1,PO2,PO3
	(ii). Explain JPEG standards in Image compression Techniques.	07	V	An	D533.5	PO1,PO2,PO3

QUESTION PAPER SETTING

The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as Presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

****

ECD610 COMPUTER HARDWARE SERVICING AND NETWORKING

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 16 weeks

Course	Instruction		Examination			
			Marks			
Computer Hardware Servicing and Networking	**Hrs/ Week**	**Hrs/ Semester**	**Internal Assessment**	**Autonomous Examination**	**Total**	**Duration**
	5	80	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

TOPICS AND ALLOCATION OF HOURS:

UNIT	TOPICS	NO. OF HOURS
I	Motherboard components and memory storage devices	15
II	I/O Devices and Interface	14
III	Trouble Shooting of Desktop and Laptops	14
IV	Computer Network Devices And OSI Layers	14
V	802.X and TCP/IP Protocols	14
	Test and Model Exam	9
TOTAL		**80**

COURSE DESCRIPTION:

Maintaining and servicing the computers, laptops and peripherals are essential requirements of the computer students. The clear understanding of computer network devices and protocols are also taught in this subject.

OBJECTIVES:

On completion of the following units of syllabus contents, the students can

- Identify the major components of CPU.
- Understand the principle of operations of all the interfacing boards, I/O Memory slots and interfacing devices.
- Know the use of diagnostic Software.
- Trouble shoot the problems in Laptop.
- Understand the different layers of OSI and their functions. Compare different LAN protocols.
- Identify the protocols used in TCP /IP and compare with OSI model. Use of IP addressing and TCP/ IP protocols briefly.

COURSE OUTCOMES

Course	**ECD610 COMPUTER HARDWARE SERVICING AND NETWORKING**
After successful completion of this course, the students should be able to	
D610.1	Familiarize about the Motherboard Components and Memory Storage devices of the computer.
D610.2	Understand the I/O devices and interface**.**
D610.3	Know the Maintenance and trouble shooting of desktop and laptops.
D610.4	Describe the functions of computer network devices and OSI layers.
D610.5	Learn about 802.X and TCP/IP protocols**,** IP addressing & Application Layer Protocols

ECD610 COMPUTER HARDWARE SERVICING AND NETWORKING

UNIT – I

MOTHERBOARD COMPONENTS AND MEMORY STORAGE DEVICES [15Hrs]

1.1 INTRODUCTION

Hardware, Software and Firmware - Mother board, [1 Hr]

IO and memory expansion slots, [1 Hr]

SMPS, Drives, front panel and rear panel connectors. [1 Hr]

1.2 PROCESSORS

Architecture and block diagram of multicore Processor, [2 Hrs]

Features of new processor(Definition only)-chipsets (Concepts only) [1 Hr]

1.3 BUS STANDARDS

Overview and features of PCI, AGP, PCMCIA, [2 Hrs]

1.4 PRIMARY MEMORY

Introduction-Main Memory, Cache memory [2 Hrs]

DDR2 ,DDR3,DDR4 and Direct RDRAM [1 Hr]

1.5 SECONDARY STORAGE

Hard Disk – Construction – Working Principle – [1 Hr]

Specification of IDE, Ultra ATA, Serial ATA

HDD Partition – Formatting, SSD Introduction [1 Hr]

1.6 REMOVABLE STORAGE

CD-R,CD-RW; DVD-ROM, DVD-RW

Construction and reading & writing operations, Zip Drive Blu-ray:

Introduction – Disc Parameters [2 Hrs]

UNIT II

I/O DEVICES AND INTERFACE [14 Hrs]

2.1 KEYBOARD

Keyboard – Signals – operation of membrane and mechanical keyboards - [2 Hrs]

Troubleshooting , Wireless keyboard.

2.2 MOUSE

Types, connectors, operation of optical mouse and troubleshooting [2 Hrs]

2.3 PRINTERS

Introduction – Types of printers, Dot matrix, Inkjet, Laser, [2 Hrs]

MFP (Multi Function Printer) and Thermal printer - Operation –Construction and

Features - Troubleshooting [1 Hr]

2.4 I/O PORTS

Serial, Parallel, USB, Game Port, and HDMI. [1 Hr]

2.5 DISPLAYS

Principles of LED(OLED, AMOLED, POLED), LCD and TFT Displays. [1 Hr]

2.6 GRAPHIC CARDS

VGA and SVGA card. [1 Hr]

2.7 MODEM

Working principle. [1 Hr]

2.8 POWER SUPPLY

Servo Stabilizers, online and offline UPS – working principles; [2 Hrs]

SMPS: Principles of operation and Block Diagram of ATX Power Supply,

Connector Specifications. [1 Hr]

UNIT III

MAINTENANCE AND TROUBLE SHOOTING OF DESKTOPAND LAPTOPS [14 Hrs]

3.1 BIOS –SETUP

Standard CMOS setup, Advanced BIOS setup, Power management [1 Hr]

Advanced chipset features, PC Bios communication – upgrading BIOS,

Flash BIOS – setup [1 Hr]

3.2 POST

Definition – IPL hardware – POST Test sequence – beep codes [2 Hrs]

3.3 DIAGNOSTIC SOFTWARE AND VIRUSES

Computer Viruses – Precautions –Anti-virus Software –identify the signature [2 Hrs]

of viruses – Firewalls and latest diagnostic softwares.

3.4 LAPTOP

Types of laptop – block diagram – working principles–configuring laptops and power settings. [1 Hr]

SMD components, ESD and precautions [1 Hr]

3.5 LAPTOP COMPONENTS

Adapter – types, Battery – types [1 Hr]

Laptop Mother Board - block diagram, Laptop Keyboard &Touchpad [1 Hr]

3.6 INSTALLATION AND TROUBLE SHOOTING

Formatting, Partitioning and Installation of OS – Trouble Shooting [2 Hrs]

Laptop Hardware problems – Preventive-maintenance techniques for laptops. [2 Hrs]

UNIT IV

COMPUTER NETWORK DEVICES AND OSI LAYERS [14 Hrs]

4.1 DATA COMMUNICATION

Components of a data communication [1 Hr]

4.2 DATA FLOW

Simplex – half duplex –full duplex [1 Hr]

4.3 TOPOLOGIES

Star, Bus, Ring, Mesh, Hybrid – Advantages and Disadvantages of each topology. [2 Hrs]

4.4 NETWORKS

Definition - Types of networks LAN – MAN – WAN – CAN – HAN – Internet –Intranet –Extranet, [3 Hrs]

Client-Server, Peer To Peer Networks. [1 Hr]

4.5 NETWORK DEVICES

Features and concepts of Switches [1 Hr]

Routers(Wired and Wireless) – Gateways**.** [2 Hrs]

4.6 NETWORK MODELS

Protocol definition - standards [1 Hr]

OSI Model – layered architecture – functions of all layers [2 Hrs]

UNIT V

802.X AND TCP/IP PROTOCOLS **[14 Hrs]**

5.1 OVERVIEW OF TCP / IP

TCP / IP – Transport Layers Protocol [2 Hrs]

Connection oriented and connectionless Services – Sockets – TCP & UDP [2 Hrs]

5.2 802.X PROTOCOLS

Concepts and PDU format of CSMA/CD (802.3) – Token bus(802.4) [1 Hr]

– Token ring (802.5) – Ethernet – Type of Ethernet (Fast Ethernet, gigabit

Ethernet) – Comparison between 802.3, 802.4 and 802.5. [2 Hrs]

5.3 NETWORK LAYERS PROTOCOL

IP –Interior Gateway Protocols (IGMP, ICMP,ARP, RARP Concept only). [2 Hrs]

5.4 IP ADDRESSING

Dotted Decimal Notation –Subnetting & Supernetting [2 Hrs]

5.5 APPLICATION LAYER PROTOCOLS

FTP– Unmanageable Switch - manageable Switch [1 Hr]

Telnet – SMTP– HTTP – DNS – POP

Introduction to cloud computing [2 Hrs]

Tests & Model Exam **[9 Hrs]**

TEXT BOOKS:

S.NO	TITLE	AUTHOR	PUBLISHER WITH EDITION
1.	Computer Installation and Servicing	D. Balasubramanian	Tata McGraw Hill Publishing Company, New Delhi – 2005
2.	IBM PC and CLONES	B.Govindrajalu	Tata McGraw Hill Publishers, New Delhi - 2001

REFERENCE BOOKS:

S.NO	TITLE	AUTHOR	PUBLISHER WITH EDITION
1.	Computer Networks	Achyut God bole	Tata Mc-GrawHil -New Delhi – 1998
2.	Principles of Wireless Networks	A unified Approach, Kaveh Pahlavan and Prashant Krishnamurty	Pearson Education, 2002
3.	Troubleshooting, Maintaining and Repairing PCs,	Stephen J Bigelow	Tata MCGraw Hill – 2001

4.	Data and Computer Communications	William Stallings	Prentice-Hall of India, Eighth Edition – 2005
5.	Upgrading and repairing laptops	Scott Mueller	QUE Publication
6.	Data Communication and Networking	Behrouz A. Forouzan	Tata MCGraw Hill – New Delhi
7.	Computer Networks	Andrew S. Tanenbaum	Prentice -Hall of India, Eighth Edition

LEARNING WEBSITES

1. https://www.academia.edu/22093398/#
2. https://abiiid.files.wordpress.com/2010/12/pc-hardware-a-beginners-guide.pdf
3. .https://www.slideshare.net/kenjoyb/k-to-12-pc-hardware-servicing-learning-module
4. https://www.techwalla.com/articles/what-is-computer-hardware-servicing
5. https://www.pdfdrive.com/computer-repair-a-complete-illustrated-guide-to-pc-hardware-e168587735.html

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO-POs &PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
D610.1	3	3	2	2	2	2	2	3	2	2
D610.2	3	3	2	2	2	2	2	3	2	2
D610.3	3	3	2	2	2	2	2	3	2	2
D610.4	3	3	2	2	2	2	2	3	2	2
D610.5	3	3	2	2	2	2	2	3	2	2
D610 Total	15	15	10	10	10	10	10	15	10	10
Correlation Level	3	3	2	2	2	2	2	3	2	2

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD620 BIO MEDICAL INSTRUMENTATION

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 16 weeks

Course	Instruction		Examination			
			Marks			
Bio medical instrumentation	**Hrs/ Week**	**Hrs/ Semester**	**Internal Assessment**	**Autonomous Examination**	**Total**	**Duration**
	5	80	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

TOPICS AND ALLOCATION:

UNIT	TOPICS	NO.OF HOURS
I	Bio-electric potentials, Electrodes and Clinical measurements	14
II	Diagnostic Instruments	15
III	Therapeutic Instruments	15
IV	Biotelemetry and Patient Safety	14
V	Modern Imaging Techniques	13
Test& Model Exam		9
TOTAL		80

COURSE DESCRIPTION:

Every year, there is a tremendous increase in the use of Modern Electronic medical equipment in the hospital and health care industry. Therefore it is necessary for every student to understand the functioning of various medical equipments.

OBJECTIVES:

After learning this subject the student will be able to understand the about

- The generation of Bio-potential and its measurement using various electrodes.
- The measurement of blood pressure.
- The measurement of lung volume.
- The measurement of respiration rate.
- The measurement of body temperature and skin temperature.
- The principle of operation of ECG recorder and the analysis of ECG waves.
- The principle of operation of EEG recorder and the analysis of EEG waves.
- The principle of operation of EMG recorder.
- The working principles of audiometer.
- The principle of operation of pacemaker.
- The basic principle of dialysis.
- The basic principle of ventilators.
- The working principles of telemetry.
- The basic principle of telemedicine.
- To learn about patient safety.
- The various methods of accident prevention.
- The basic principle of various types of lasers and their applications.
- The basic principle of various types of Medical Imaging Systems.

COURSE OUTCOMES

Course	**ECD620 BIO MEDICAL INSTRUMENTATION**
After successful completion of this course, the students should be able to	
D620.1	Understand the concepts of Bio electric potentials, Electrodes and clinical measurements.
D620.2	Learn about diagnostic instruments.
D620.3	Know therapeutic instruments.
D620.4	Aware about biotelemetry and patient safety
D620.5	Familiarize about Modern imaging techniques.

ECD620 BIO MEDICAL INSTRUMENTATION

UNIT I

BIO-ELECTRIC POTENTIALS, ELECTRODES AND CLINICAL MEASUREMENTS **[14Hrs]**

1.1 BIO POTENTIALS AND ELECTRODES

Elementary ideas of cell structure, [2 Hrs]

Bio-electric potentials and their origin [1 Hr]

Resting and action potentials [2 Hrs]

Propagation of action potential [1 Hr]

Electrodes– Micro – Skin surface– needle electrodes. [1 Hr]

1.2 CLINICAL MEASUREMENTS

Measurement of Blood pressure: Sphygmomanometer– Blood flow meter (Electromagnetic & ultrasonic blood flow meter) [2 Hrs]

Acid base balance: pH, Measurement of pH value of various body fluids [1 Hr]

Measurement of Respiration rate: Impedance Pneumograph [2 Hrs]

Measurement of Lung volume: Spiro meter– Heart rate monitor [1 Hr]

Medical laboratory equipment: Auto analyzer [1 Hr]

UNIT II

DIAGNOSTIC INSTRUMENTS **[15Hrs]**

2.1 ELECTRO- CARDIO GRAPH (ECG)

12 Lead system of ECG– ECG recorder [2 Hrs]

Analysis of abnormal ECG waves. [1 Hr]

2.2 NERVOUS SYSTEM

Electro- Enchephalo Graph (EEG) - 10-20 EEG lead system [2 Hrs]

EEG recorder - EEG wave types– Clinical uses of EEG [1 Hr]

2.3 ELECTRO– MYO GRAPH (EMG)

EMG waves– Measurement of conduction velocity [2 Hrs]

EMG recorder [1 Hr]

2.4 ELECTRO- RETINO GRAPH (ERG)

ERG recorder [2 Hrs]

ERG wave [1 Hr]

2. 5 AUDIOMETER

Principle– types – Basics audiometer working [2 Hrs]

Air conduction and bone conduction test [1 Hr]

UNIT III

THERAPEUTIC INSTRUMENTS [15 Hrs]

3.1 CARDIAC PACEMAKER

Need for Pacemaker-Classification [1 Hr]

R-wave triggered and Ventricular inhibited implantable [1 Hr]

Pace makers– Programmable pacemaker

3.2 CARDIAC DEFIBRILLATORS

Need for Defibrillator - Classification [2 Hrs]

AC and DC defibrillators [1 Hr]

3.3 HEART LUNG MACHINE :

Need for Heart Lung Machine [1 Hr]

Block diagram – working [2 Hrs]

3.4 DIALYSIS

Need for Dialysis – Processes involved in Dialysis - Hemo dialysis [2 Hrs]

Peritoneal dialysis - Comparison of Hemo dialysis and Peritoneal dialysis [1 Hr]

3.5 LITHITRIPSY

Need for Lithotriptor- block diagram and working [2 Hrs]

3.6 VENTILATORS

Need for Ventilators - Types – modern ventilator block diagram– Working [2 Hrs]

UNIT IV

BIOTELEMETRY AND PATIENT SAFETY [14 Hrs]

4.1 BIOTELEMETRY

Physiological parameters adaptable to biotelemetry [1 Hr]

Components of a biotelemetry system [1 Hr]

Applications of biotelemetry [1 Hr]

Radio telemetry with sub carrier: single channel and [1 Hr]

multi channel telemetry system

Telemedicine: concept and applications. [1 Hr]

4.2 PATIENT SAFETY

Physiological effects of electric current [1 Hr]

Micro and macro shock–Hazardous situations of

micro and macro shocks- [2 Hrs]

leakage current– lethal effects of leakage current [1 Hr]

4.3 METHODS OF ACCIDENT PREVENTION

Grounding – Double Insulation [1 Hr]

Ground fault circuit interrupter (GFI) [1 Hr]

Safety aspects in electro surgical units: burns High frequency [2 Hrs]

Current hazard-explosion hazard.

Precautions to minimize electric shock hazards [1 Hr]

UNIT V

MODERN IMAGING TECHNIQUES **[13Hrs]**

5.1 : Laser

Laser beam properties– Block diagram and explanation of [2 Hrs]

ND -Yag LASER –Applications of LASER inpatient care. [2 Hrs]

5.2 : X ray

Properties of X-Rays - Working of X ray apparatus– Special techniques [2 Hrs]

in X-ray imaging

C arm image intensifier- Computerized Axial tomography [2 Hrs]

– CT scanner- Angiography

5.3 : Ultrasonic imaging techniques:

Pulse echo system - Echo Cardiography [1 Hr]

Operating modes – Working [2 Hrs]

5.4 : Magnetic Resonance Imaging techniques

Working [1 Hr]

Superiority of MRI Scan, Positron Emission Tomography [1 Hr]

Tests& Model Exam **[9 Hrs]**

TEXT BOOKS:

S.NO	TITLE	AUTHOR	PUBLISHER WITH EDITION
1.	Bio medicaI Instrumentation and measurements	Leslie Cromwell– Fredj. Wibell, Erich A.PFeither	II Edition Jacobson and Webstar–Medicine and clinical Engineering
2.	Handbook of Biomedical Instrumentation	R.S. Khandpur	McGraw Hill Education

REFERENCE BOOKS:

S.NO	TITLE	AUTHOR	PUBLISHER WITH EDITION
1.	Medical Electronics	Kumara doss	--
2.	Introduction to Medical Electronics	B.R. Klin	Foulsham-Tab Ltd
3	Introduction to Biomedical Instrumentation	Mandeep Singh	Printice Hall India2010.

LEARNING WEBSITES

1.https://www.pdfdrive.com/biomedical-instrumentation-e51899426.html

2.https://biomedical-engineering-online.biomedcentral.com/

3. https://www.pdfdrive.com/biomedical-instrumentation-and-measurements-e186986101.html

4.https://www.electrical4u.com/introduction-to-biomedical-instrumentation/

5.https://en.wikipedia.org/wiki/Bioinstrumentation

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	-	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
D620.1	3	3	2	2	2	2	2	3	2	2
D620.2	3	3	2	2	2	2	2	3	2	2
D620.3	3	3	2	2	2	2	2	3	2	2
D620.4	3	3	2	2	2	2	2	3	2	2
D620.5	3	3	2	2	2	2	2	3	2	2
D620 Total	15	15	10	10	10	10	10	15	10	10
Correlation Level	3	3	2	2	2	2	2	3	2	2

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

****

ECD631 TELEVISION ENGINEERING

TEACHING AND SCHEME OF EXAMINATION:

No. of weeks per semester: 16 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/ Week	Hrs / Semester	Internal Assessment	Autonomous Examination	Total	
Television Engineering	5	80	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

TOPICS AND ALLOCATION OF HOURS:

UNIT	TOPICS	NO. OF HOURS
I	Television Fundamentals	15
II	Camera Tubes and Picture Tubes	14
III	Television Transmitter and Television Receiver	15
IV	Modern Television Technology	14
V	Advanced Television Systems.	13
	Test & Model Exam	9
TOTAL		**80**

COURSE DESCRIPTION:

This course makes the students to understand from the basic concepts of TV to advanced techniques of TV. It also enables the students to have the knowledge about the Modern Technology including flat panel display. This course makes the students to understand about Color TV fundamentals .The subject also introduces troubleshooting techniques. It gives the clear understanding about TV standards.

OBJECTIVES:

On completion of the syllabus, the students must be able to

- Understand CVS and CCVS signal.
- Understand the different types of scanning.
- Study the types of camera tubes and picture tubes.
- Explain about TV transmitter and TV receiver (Monochrome and PAL).
- Study the Modern TV technology.
- Understand the use of Advanced TV systems.

COURSE OUTCOMES

Course	**ECD631 TELEVISION ENGINEERING**
After successful completion of this course, the students should be able to	
D 631.1	Familiarize about monochrome and colour T.V fundamentals.
D 631.2	Learn about the working principle of the Camera Tubes and Picture Tubes.
D 631.3	Understand the concepts of TV transmitter and TV receiver.
D 631.4	Know the modern Television Technology.
D 631.5	Understand about advanced television systems .

ECD631 TELEVISION ENGINEERING

UNIT I

TV FUNDAMENTALS **[15 Hrs]**

1.1 MONOCHROME TV:

Basic block diagram of Monochrome TV transmitter and Receiver [1 Hr]

Scanning process – horizontal , vertical and sequential scanning [1 Hr]

flicker – interlaced scanning (qualitative treatment only) [1 Hr]

need for synchronization – blanking pulses – Aspect ratio [1 Hr]

Resolution – vertical and horizontal resolution [1 Hr]

video bandwidth – composite video signal (CVS) [1 Hr]

Definitions for Vertical sync pulse, Serrated vertical pulse, [1 Hr]

Equalizing pulse Positive & Negative modulation-TV Standards [1 Hr]

1.2 COLOR T.V. FUNDAMENTALS:

Additive mixing of colours [1 Hr]

color perception – Chromaticity diagram [2 Hrs]

Definition for Luminance, Hue Saturation and Chrominance [2 Hrs]

Formation of chrominance signal in PAL system with weighting factors. [1 Hr]

Colour composite video signal(CCVS). [1 Hr]

UNIT II

CAMERA TUBES AND PICTURE TUBES **[14 Hrs]**

2.1 CAMERA TUBE :

Characteristics -Types of camera tube [2 Hrs]

working principle of Vidicon camera tube-study of Target plate (only) of Plumbicon camera tube [2 Hrs]

CCD camera -Video processing of camera pick up signal [2 Hrs]

Block diagram and Principle of working of colour TV camera tube. [1 Hr]

2.2 PICTURE TUBE :

Magnetic deflection and Electrostatic focusing [1 Hr]

screen phosphor – screen burn – screen Persistance- [2 Hrs]

Aluminized screen- Types of color picture tubes construction and working [2 Hrs]

Principle of Trinitron colour picture tube - Automatic degaussing [2 Hrs]

UNIT III

TELEVISION TRANSMITTER AND RECEIVER

3.1 TELEVISION TRANSMITTER [15 Hrs]

Types- Comparison-Principle- Block diagram of Low level [1 Hr]

IF Modulated TV transmitter [1 Hr]

Visual Exciter - Aural Exciter [1 Hr]

principle of working of CIN Diplexer [1 Hr]

color compatibility [1 Hr]

PAL colour coder working operation [1 Hr]

Merits and demerits of PAL system [1 Hr]

3.2 TELEVISION RECEIVER

Block diagram of monochrome receiver- Functions of each block [2 Hrs]

Need for AGC- merits of AGC [1 Hr]

Video amplifier requirements [1 Hr]

High and Low frequency compensation [1 Hr]

Block diagram of PAL color Receiver -Need for sync separator [1 Hr]

Basic sync separator circuits –Integrator and Differentiator [1 Hr]

AFC –need for AFC, Horizontal AFC [1 Hr]

UNIT IV

MODERN TELEVISION TECHNOLOGY [14 Hrs]

MODERN TV

Flat panel Display-Principles of operation-Large screen display [2 Hrs]

Types of TV-projection TV-plasma TV-merits of plasma TV [2 Hrs]

construction and working operation of LCD TV [2 Hrs]

LED TV -Types of LED TV -working operation of LED TV [2 Hrs]

-merits of LED TV

LCD projector working operation [1 Hr]

set top box-principles of DTH-Trouble shooting of set top box [2 Hrs]

communication cables-Types-Feeder wire-coaxial cable [2 Hrs]

and optical fiber cable

RF TV Tuner card. [1 Hr]

UNIT V

ADVANCED TELEVISION SYSTEMS **[13Hrs]**

5.1 ADVANCED TV

Block diagram of a digital color TV receiver [2 Hrs]

Remote control IR transmitter and receiver - Closed circuit TV system [2 Hrs]

Applications of CCTV –scrambler-necessity [1 Hr]

basic principle-types Descrambler block diagram Telecine equipment [2Hrs]

Digital CCD Tele cine system [1 Hr]

Introduction to High definition TV(HDTV) & 3DTV. [2 Hrs]

5.2:TV CONNECTOR PORTS

HDMI port-USB port [2 Hrs]

RF in-AV Jack. [1 Hr]

Tests & Model Exam **[9 Hrs]**

TEXT BOOKS:

S.No	Title	Author	Publisher with Edition
1.	Modern Television Practice-Transmission, Reception, Applications	R.R.Gulati	New Age Publishers -Fifth Edition – 2015
2.	TV & Video Engineering	A.M.Dhake	Tata MCGraw Hill- Second Edition-2003

REFERNCEBOOKS:

S.No	Title	Author	Publisher with Edition
1.	Monochrome & color TV	R.R.Gulati	New Age publishers -2003
2.	Colour TV theory and practice	S.P.Bali	Tata MCGraw Hill- 1994
3.	Modern VCD- video CD player introduction, servicing and trouble shooting	Manohar lotia & Pradeep Nair	BPB Publications-2002

LEARNING WEBSITES

1. https://www.pdfdrive.com/monochrome-and-colour-television-rrgulati-d31146632.html
2. https://www.pdfdrive.com/lcd-led-tv-panels-modification-and-major-repairs-e48676743.html
3. https://www.pdfdrive.com/led-tv-service-manual-lcd-television-repaircom-e17350712.html
4. https://harshasnmp.files.wordpress.com/2017/11/monochrome-and-colour-television-r-r-gulati.pdf

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	-	**25 Marks**

CO-POs &PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
D631.1	3	3	2	2	2	2	2	3	2	2
D631.2	3	3	2	2	2	2	2	3	2	2
D631.3	3	3	2	2	2	2	2	3	2	2
D631.4	3	3	2	2	2	2	2	3	2	2
D631.5	3	3	2	2	2	2	2	3	2	2
D631Total	15	15	10	10	10	10	10	15	10	10
Correlation Level	3	3	2	2	2	2	2	3	2	2

Correlation level 1- Slight (low)
Correlation level 2- Moderate (Medium)
Correlation level 3- Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

****

ECD632 MOBILE AND OPTICAL COMMUNICATION

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 16 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/ Week	Hrs / Semester	Internal Assessment	Autonomous Examination	Total	
Mobile and Optical Communication	5	80	25	100*	100	3 Hrs

*** Examination will be conducted for 100 marks and it will be reduced to 75marks.**

TOPICS AND ALLOCATION OF HOURS:

UNIT	TOPICS	NO. OF HOURS
I	Mobile Communication concepts	14
II	Equalization, Diversity, Channel coding and Speech coding	14
III	Wireless Networking , Personal Communication Services/ Networks(PCS/PCNS) and Network databases	15
IV	Optical Cables, Connectors, Splicers, Optical Digital and Analog link	14
V	WDM Concepts and Components	14
Tests and Model Exam		9
TOTAL		**80**

COURSE DESCRIPTION:

Communication is one of the integral parts of science that has always been a focus point for exchanging information among parties at locations physically apart. After its discovery, telephones have replaced the telegrams and letters. Similarly, the term ‘mobile’ has completely revolutionized the communication by opening up innovative applications that are limited to one’s imagination. Today, mobile communication has become the backbone of the society. All the mobile system technologies have improved the way of living. Usually Mobile cellular networks have both Circuit Switching and Packet Switching for handling calls. For Circuit Switching Optical fiber using WDM is employed. Hence in this subject, with Mobile communication, Optical communication is added.

OBJECTIVES:

On completion of the following units of syllabus contents, the students must be able to:

- Know the concept of Mobile Communication.
- Know the concept of Channel Assignments.
- Know about the Handoff processes performed in Mobile Communication.
- Know the interferences and system capacity.
- Know the methods of improving coverage and capacity to avoid network congestion.
- Know the concept of equalization, diversity , channel coding and speech coding.
- Know the concept of LTE and VoLTE (Voice over Long Term Evolution.
- Know about wireless networking , Personal Communication Services/ Networks(PCS/PCNS) and network databases.
- Know about Universal Mobile Telecommunication System (UMTS).
- Know about Fiber optic cables.
- Know about Power launching and coupling.
- Know about Fiber-to-fiber joints.
- Know about Fiber splicing techniques.
- Know about Optical fiber connectors.
- Know about Digital transmission systems.
- Know about WDM concepts and components.
- Know about Optical networks.

COURSE OUTCOMES

Course	**ECD632 Mobile and optical communication**
After successful completion of this course, the students should be able to	
D632.1	Familiarize about Mobile communication concepts.
D632.2	Know about Equalization, Diversity channel coding ,speech coding ,LTE and VoLTE.
D632.3	Understand the concepts of Wireless Networking and personal communication services (PCS/PCNs) and Data Networks
D632.4	Acquire knowledge on optical communication.
D632.5	Explain about WDM concepts and components.

ECD632 MOBILE AND OPTICAL COMMUNICATION

UNIT I

MOBILE COMMUNICATION **[14 Hrs]**

1.1 CELLULAR CONCEPTS

Channel Assignment strategies [3 Hrs]

1.2 HAND OFF STRATEGIES

Prioritizing Handoffs- [1 Hr]

Practical Handoff Considerations [2 Hrs]

1.3 INTERFERENCE AND SYSTEM CAPACITY

Co-channel interference and System Capacity [1 Hr]

Channel Planning for wireless Systems [1 Hr]

Adjacent Channel Interference [1 Hr]

Power Control for Reducing Interference [1 Hr]

1.4 IMPROVING COVERAGE AND CAPACITY

Cell splitting and Cell sectoring [1 Hr]

Repeaters for Range Extension [1 Hr]

Micro cell Zone Concept [2 Hrs]

UNIT II

EQUALIZATION, DIVERSITY, CHANNEL CODING AND SPEECH CODING **[14 Hrs]**

2.1 FUNDAMENTALS OF EQUALIZATION

Introduction Training a Generic Adaptive Equalizer- Equalizers in

Communication Receiver [2 Hrs]

Survey of Equalization Techniques [1 Hr]

2.2: DIVERSITY TECHNIQUES

Practical considerations in space diversity – Polarization diversity – [2 Hrs]

Frequency diversity – Time diversity – RAKE Receiver - Interleaving. [1 Hr]

2.3: FUNDAMENTALS OF CHANNEL CODING [2 Hrs]

2.4: SPEECH CODING

Introduction – Characteristics of Speech signals – [1 Hr]

Probability Density Function – Autocorrelation function – [1 Hr]

Frequency Domain Coding of Speech – Sub band Coding – [1 Hr]

Adaptive Transform Coding – Vocoders – The GSM Codec. [1 Hr]

2.5: LTE AND VoLTE (voice over long term evolution) **[** 2 Hrs]

UNIT III

WIRELESS NETWORKING, PERSONAL COMMUNICATION SERVICES/ NETWORKS (PCS/PCNs) AND NETWORK DATA BASES **[15 Hrs]**

3.1 INTRODUCTION TO WIRELESS NETWORKS [2 Hrs]

3.2 DIFFERENCE BETWEEN WIRELESS NETWORKS AND FIXED NETWORKS

Limitations in wireless networking, Merging wireless network and [2 Hrs]

PSTN Development of Wireless Networks [1 Hr]

3.3 WIRELESS DATA SERVICES

Cellular Digital Packet Data (CDPD) [1 Hr]

Advanced Radio Data Information Systems (ARDIS) [1 Hr]

RAM Mobile Data (RMD) [1 Hr]

3.4 PERSONAL COMMUNICATION SERVICES/ NETWORKS (PCS/PCNS)

Packet Vs Circuit Switching for PCN [2 Hrs]

Cellular Packet Switched Architecture [1 Hr]

3.5 NETWORK DATABASES

Distributed Database for Mobility Management [2 Hrs]

3.6 UNIVERSAL MOBILE TELECOMMUNICATION SYSTEM (UMTS) [2 Hrs]

UNIT IV

OPTICAL COMMUNICATION **[14 Hrs]**

4.1: FIBER OPTIC CABLES [2 Hrs]

4.2: POWER LAUNCHING AND COUPLING

Source to Fiber Power Launching - Source Output Pattern- [1 Hr]

Schematic diagram of an optical source coupled to an optical fiber- [1 Hr]

Lensing scheme for coupling improvement [1 Hr]

4.3: FIBER-TO-FIBER JOINTS [1 Hr]

4.4 : FIBER SPLICING TECHNIQUES

4.5 :OPTICAL FIBER CONNECTORS [2 Hrs]

4.6 : DIGITAL TRANSMISSION SYSTEMS

Simplex point to point transmission link [2 Hrs]

– System consideration [1 Hr]

4.7 : ANALOG TRANSMISSION SYSTEMS

Over view of Analog links [3 Hrs]

UNIT V

WDMCONCEPTS AND COMPONENTS [14Hrs]

1.1 : OPERATIONAL PRINCIPLES OF WDM [2 Hrs]

1.2 : WDM COMPONENTS

2x2 Fiber couplers - Star matrix representation – [1 Hr]

2x2 Waveguide couplers – Star couplers [1 Hr]

1.3 : OPTICAL NETWORKS

Basic Networks - Network topologies – [1 Hr]

Performance of Star Architecture [1 Hr]

1.4 : SONET / SDH

Basic concepts - Transmission Formats and Speeds – Optical Interfaces – [1 Hr]

SONET/SDH rings - SONET/SDH Networks [1 Hr]

1.5 : WAVELENGTH - ROUTED NETWORKS

Optical Cross – connects [2 Hrs]

1.6 : OPTICAL CDMA [2 Hrs]

1.7 : ULTRAHIGH CAPACITY NETWORKS

Ultrahigh Capacity WDM Systems – [1 Hr]

Bit- interleaved Optical TDM-Time-Slotted Optical TDM [1 Hr]

Tests & Model Exam [9 Hrs]

TEXT BOOKS

SL.No	Title	Author	Publisher with Edition
1.	Wireless Communications Principles and Practice	Theodore S. Rappaport	Pearson Education, 2003
2.	Mobile Communications	Jochen Schiller	Pearson Education, 2009, Second edition

REFERENCE BOOKS

SL. No	Title	Author	Publisher with Edition
1.	Wireless Communication Principle and Practice	Theodore S.Rappaport	Pearson Education, 2003
2.	Mobile Cellular Communication	Jochen Schiller	PearsonEducation, 2009,Second edition
3.	Optical fiber communication	Gerd Keiser	Third Edition – McGraw Hill-2000
4.	Mobile Cellular Communications	W.C.Y. Lee	2nd Edition, MC Graw Hill, 1995

LEARNING WEBSITES

1.https://www.pdfdrive.com/wireless-and-mobile-communications-e10339327.html

2. https://www.pdfdrive.com/introduction-to-mobile-network-engineering-gsm-3g-wcdma-lte-and-teh-road-to-5g-d188626922.html

3. https://www.pdfdrive.com/5g-mobile-communications-d158209927.html

4. https://www.pdfdrive.com/handbook-of-fiber-optic-data-communication-third-edition-a-practical-guide-to-optical-networking-d177047081.html

5. https://www.pdfdrive.com/fiber-optic-communication-systems-d29302044.html

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	-	**25 Marks**

CO-POs &PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
D632.1	3	3	2	2	2	2	2	3	2	2
D632.2	3	3	2	2	2	2	2	3	2	2
D632.3	3	3	2	2	2	2	2	3	2	2
D632.4	3	3	2	2	2	2	2	3	2	2
D632.5	3	3	2	2	2	2	2	3	2	2
D632Total	15	15	10	10	10	10	10	15	10	10

Correlation Level	3	3	2	2	2	2	2	3	2	2

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high**)**

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy .The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

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Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

******

ECD633 EMBEDDED SYSTEMS

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 16 Weeks

Course	Instruction		Examination			
	Hrs/ Weeks	Hrs/ Semester	Marks			Duration
			Internal Assessment	Autonomous Examination	Total	
Embedded Systems	5	80	25	100*	100	3 Hrs

*** Examination will be conducted for 100 marks and it will be reduced to 75 marks.**

TOPICS AND ALLOCATION OF HOURS:

UNIT	TOPIC	NO.OF HOURS
I	Introduction to Embedded systems and ARM processor	16
II	ARM instruction set	15
III	LPC 2148 controller	15
IV	LPC 2148 peripherals	15
V	Operating System	10
Test & Model Exam		9
Total		**80**

COURSE DESCRIPTIPN:

This course makes the students to understand the definition for Embedded Systems. It also enables the students to have the knowledge about the different architectures, RISC and CISC processors. This subject makes the students to understand about RTOS. To specific, the subject deals with ARM7 RISC processor and the on chip peripherals of LPC2148.

OBJECTIVES:

On completion of the syllabus, the students must be able to

- Understand ARM7 processor .
- Understand the architecture of LPC 2148.
- Understand ARM7 instruction set.
- Understand the types of buses.
- Explain On chip peripherals.
- Have clear knowledge about RTOS concepts.

COURSE OUTCOMES

Course	**ECD633 EMBEDDED SYSTEMS**
After successful completion of this course, the students should be able to	
D633.1	Familiarize about Introduction to Embedded Systems and ARM Processor.
D633.2	Know about ARM Instruction Set.
D633.3	Understand the concepts of LPC 2148 Controller.
D633.4	Acquire knowledge on LPC 2148 Peripherals.
D633.5	Explain about Operating System- Embedded OS and RTOS.

ECD633 EMBEDDED SYSTEMS

UNIT I

INTRODUCTION TO EMBEDDED SYSTEMS AND ARM PROCESSOR [16 Hrs]

1.1 EMBEDDED SYSTEMS

Definition of Embedded System [1 Hr]

Features of Embedded System -Types of Embedded System [2 Hrs]

List of Embedded System Devices [2 Hrs]

Harvard and Von-Neumann architectures [2 Hrs]

RISC and CISC Processors. [1 Hr]

1.2 ARM PROCESSOR ARCHITECTURE FUNDAMENTALS

Block diagram of ARM based embedded system [2 Hrs]

with hardware components

Pipeline-Data Flow Model-CPU registers – Modes of Operation [2 Hrs]

PSW -Processor State and Instruction Set-Exceptions [2 Hrs]

Interrupts-Vector table-Little Endian and Big Endian. [2 Hrs]

UNIT II

ARM INSTRUCTION SET [15 Hrs]

2.1 INSTRUCTION SETS

ARM state instruction set-Thumb state Instruction Sets(Brief introduction only), [2 Hrs]

Data Processing Instructions, [2 Hrs]

Branch Instructions, Load-Store Instructions [2 Hrs]

Software Interrupt Instruction, Program Status Register [3 Hrs]

Instructions, Stack Instructions, Conditional Execution [3 Hrs]

2.2 SIMPLE PROGRAM:

Addition, Subtraction using ARM processor assembly language. [1 Hr]

Multiplication using ARM processor assembly language [2 Hrs]

UNIT III

LPC 2148 CONTROLLER [15 Hrs]

3.1 INTRODUCTION TO LPC 2148 ARMCONTROLLER

LPC 2148 ARM Controller - Features-Block diagram [2 Hrs]

Memory and on chip peripheral devices [2 Hrs]

ARM 7 TDMI-S Nomenclature [1 Hr]

Memory Map – Memory re-map and boot block [2 Hrs]

Types of buses. [1 Hr]

3.2 SYSTEM CONTROL FUNCTIONS

Crystal oscillator-PLL - Power control [2 Hrs]

Reset – VPB divider – Wakeup Timer [2 Hrs]

Vector Interrupt controller-(VIC) [2 Hrs]

Register description-External Interrupts. [1 Hr]

UNIT IV **[15 Hrs]**

LPC 2148 PERIPHERALS

4.1: PERIPHERALS

Pin connect block-Features-pin connect block register description [2 Hrs]

GPIO (Slow)- Features-register description [2 Hrs]

Timer/Counter- Block diagram-Register description [2 Hrs]

PWM-features-register description [2 Hrs]

ADC -features- register description [1 Hr]

DAC-features-register description [1 Hr]

4.2: SERIAL COMMUNICATION IN LPC 2148

UART features [2 Hrs]

UART0 Block diagram [2 Hrs]

UART0 register description. [1 Hr]

UNIT V

OPERATING SYSTEM **[10 Hrs]**

EMBEDDED OS AND RTOS

Introduction to OS-Functions of OS [1 Hr]

Embedded OS [1 Hr]

Foreground/background systems [1 Hr]

Real time system concepts [1 Hr]

Resources-shared resources-Critical section [1 Hr]

Multitasking-Tasks-kernel- Scheduler-Round Robin [1 Hr]

Non Pre-emptive and Pre-emptive scheduling [1 Hr]

Context switch- re-entrancy- task priorities- Event flag [1 Hr]

mutual exclusion-semaphores and types [1 Hr]

Message mail box-Message Queues. [1 Hr]

Tests & Model Exam [9 Hrs]

TEXT BOOKS:

S.No	Title	Author	Publisher with Edition
1.	Microprocessor & Microcontroller	B.P.Singa	Reprint-Galgotia Publication Pvt Ltd., - 2001
2.	Real Time Concepts for Embedded Systems	Qing Li and Caroline Yao	Elsevier publication- 2003

REFERENCE BOOKS:

S.No	Title	Author	Publisher with Edition
1.	ARM System Developer's Guide Designing and Optimizing	Andrew N.Sloss	Elsevier publication- 2004
2	Embedded Systems	B.Kanta Rao	PHI publishers Eastern Economy Edition, 2011
3.	Embedded Systems Architecture	Tammy Noergaard	Newness Edition
4.	ARM System- On-Chip Architecture	Steve Furbe	Pearson Education Second Edition - 2000
5.	Embedded Real Time Systems	Dr. K.V.K.K Prasad	Dream tech press,2009

LEARNING WEBSITES

1. https://www.pdfdrive.com/arm-system-on-chip-architecture-d158396561.html

2.https://www.pdfdrive.com/arm-system-developers-guide-e33462626.html

3.https://www.pdfdrive.com/arm-assembly-language-programming-and-architecture-e158008271.html

4.https://www.pdfdrive.com/microc-os-ii-the-real-time-kernel-e183919184.html

5.https://www.pdfdrive.com/programming-embedded-systems-second-edition-with-c-and-e10463044.html

CONTINUOUS INTERNAL ASSESSMENT

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ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	-	**25 Marks**

CO-POs &PSOs MAPPING MATRIX

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D633.2	3	3	2	2	2	2	2	3	2	2
D633.3	3	3	2	2	2	2	2	3	2	2
D633.4	3	3	2	2	2	2	2	3	2	2
D633.5	3	3	2	2	2	2	2	3	2	2
D633Total	15	15	10	10	10	10	10	15	10	10
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Correlation level 1- Slight (low)
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QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

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ECD640 COMPUTER HARDWARE SERVICING AND NETWORKING PRACTICAL

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester: 16 Weeks

Course	Instruction		Examination			
			Marks			
	Hrs/ Week	Hrs/ Semester	Internal Assessment	Autonomous Examination	Total	Duration
Computer Hardware Servicing and Networking Practical	6	96	25	100*	100	3Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

DETAILED ALLOCATION OF MARKS

S.No	DESCRIPTION	MAX. MARKS	
		Part A	Part B
1	PROCEDURE	15	15
2	EXECUTION	20	20
3	RESULT WITH PRINTOUT	05	05
4	VIVA–VOCE	10	
5	MINI PROJECT	10	
	TOTAL	**100**	

Mini Project Evaluation (10 marks)

Breakup Details

1	Project Description	05
2	Project Demo	05
	Total	**10**

COURSE DESCRIPTION

The course aims at making the students familiar with various parts of computers and laptops and how to assemble them and the different types of peripherals desired. In addition, the course will provide the students with necessary knowledge and skills in computer and laptop software installation and maintenance and to make him diagnose the software faults. This subject also gives the knowledge and

competency to diagnose the problems in computer hardware and peripherals and gives the knowledge for trouble shooting for systematic repair and maintenance of computers and laptops

HARDWARE REQUIRED: (FOR A BATCH OF 30 STUDENTS)

S.No	Name of The Equipment	Required Nos
1	Computer with Pentium/ Core processors with inbuilt NIC	30 Nos
2	Hard disk drive	02 Nos
3	CD / DVD Writer	02 Nos
4	Blu Ray writer	01 No
5	Blank DVD,Blu-ray disk	30 Nos
6	Web camera	02 Nos
7	Laser Printer	02 Nos
8	Dot matrix Printer	02 Nos
9	Blank DVD	30 Nos
10	Scanner	02 Nos
11	Laptop	02 Nos
12	Biometric device	02 Nos
13	Crimping Tool	06 Nos
14	Network Cables	--
15	RJ45Tester	06 Nos
16	Modem with internet connection	02 Nos
17	Hub	02 Nos
18	Switch 2x2/4x4	02 Nos
19	Router	02 Nos

SOFTWARE REQUIRED: (FOR A BATCH OF 30 STUDENTS)

S.No	Name of The Software	Required Nos
1.	Windows XP operating system	15
2.	Windows 7 OS	15
3.	DVD/ CD Burning S/W (Ahead Nero or latest S/W)	30

OBJECTIVES:

On completion of the following exercises, the students must be able to

- Know the various indicators, switches, SMPS, mother board, connectors and various disk drivesused in Computers.
- Install various secondary storage devices with memory partition and formatting.
- Acquire the practical knowledge about the installation of various devices like printer, scanner, web camera and bio-metric devices.
- Assemble PC system and laptop and checking
- Install Dual OS in a system.
- Enable to perform different cabling in a network.
- Configure Internet connection and able to debug network issues.
- Develop the Mini Project.

COURSE OUTCOMES

Course	**ECD640 COMPUTER HARDWARE SERVICING AND NETWORKING PRACTICAL**
After successful completion of this course, the students should be able to	
D640.1	Familiarize about identification of system layout, installation of hard disk and DVD/BLU-ray writer and assemble a system with an add on cards.
D640.2	Install and configure printer, Scanner , Web cam and bio-metric device.
D640.3	Install OS and Dual OS in the assembled system and assemble and disassemble a Laptop to identify the parts and install the different drives.
D640.4	Do the Cabling works for establishing a network, Crimp the network cable with RJ 45 connector and test the crimped cable using a cable tester and interface two PCs to form Peer To Peer network using the connectivity devices Switch or Router in a LAN.
D640.5	Share the files, folders, printer in a LAN, Configure DNS, Install and configure Network Devices: HUB, Switch or Routers NIC, Install and configure a DHCP server and Connect the computer in local area network and Develop mini project with report.

ECD640 COMPUTER HARDWARE SERVICING AND NETWORKING PRACTICAL

PART A – COMPUTER HARDWARE SERVICING

1. IDENTIFICATION OF SYSTEM LAYOUT

i) Identify front panel indicators & switches and Front side & rear side connectors.

ii) Familiarize the computer system layout by marking positions of SMPS, Motherboard, FDD, HDD, CD, DVD and add on cards.

2. HARD DISK

i) Configure bios setup program and troubleshoot the typical problems using BIOS utility.

ii) Install, Configure, Partition and Format Hard disk.

3. DVD/BLU-RAY WRITER

i) Install and Configure a DVD Writer and record a blank DVD.

ii) Install and Configure a Blu-ray Writer and record a blank Blu-ray Disc.

4. Printer Installation

i) Install and configure Dot matrix printer.

ii) Install and configure Laser printer.

5. i) Install and configure Scanner.

ii) Install and configure Web cam and bio-metric device.

6. i) Assemble a system with add on cards and check the working condition of the system.

ii) Install OS in the assembled system.

7. Install Dual OS in a system.

8. i) Assemble and Disassemble a Laptop to identify the parts.

ii) Installation of different device drives and installation of different applications software.

PART B – COMPUTER NETWORKING

9. Do the following Cabling works for establishing a network.

i) Crimp the network cable with RJ 45 connector in Standard cabling mode and cross cabling mode.

ii) Test the crimped cable using a cable tester.

10. Use IPCONFIG, PING , TRACERT and NETSTAT utilities to debug the network issues.

11. Interface two PCs to form Peer To Peer network using the connectivity devices Switch or Router in a LAN .

12. (i) Share the files and folders in a LAN.

(ii)Share a printer in a LAN.

13. Remote Desktop, Remote Assistance, Telnet, HyperTerminal, Team Viewer.

14. Configure DNS to establish interconnection between systems and describe how a name is mapped to IP Address.

15. i) Install and configure Network Devices: HUB, Switch(4/8/24Ports), Routers

    ii) Install and Configure NIC.

16. Installation and configuration of DHCP server.

17. Mini Project

The mini project is activity based and it may be given to group of maximum of six students for hands on experience and to create scientific temper

LEARNING WEBSITES

1. https://www.academia.edu/22093398/computer_hardware_servicing_ict-computer_hardware_servicing
2. https://www.pdfdrive.com/computer-repair-a-complete-illustrated-guide-to-pc-hardware-e168587735.html
3. https://www.pdfdrive.com/laptop-repair-complete-guide-including-motherboard-component-level-repair-e168477884.html
4. https://gwptck.ac.in/admin/filemanager/files/3259%20-%20%20BASICS%20OF%20CHN%20LAB.pdf
5. https://youtu.be/z2lZhi9jK0o?t=3

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:

a) Attendance (Award of marks same as theory courses)	:	05 Marks
b) Procedure/ observation and tabulation/ Other Practical related Work	:	05 Marks
c)Tests	:	10 Marks
d) Student Centered Learning (SCL) work sheet	:	05 Marks
Total		25 Marks

CO-POs &PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
D640.1	3	3	3	3	3	3	3	3	3	3
D640.2	3	3	3	3	3	3	3	3	3	3
D640.3	3	3	3	3	3	3	3	3	3	3
D640.4	3	3	3	3	3	3	3	3	3	3
D640.5	3	3	3	3	3	3	3	3	3	3
D640Total	15	15	15	15	15	15	15	15	15	15
Correlation Level	3	3	3	3	3	3	3	3	3	3

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

ECD640 COMPUTER HARDWARE SERVICING AND NETWORKING PRACTICAL

MODEL QUESTION PAPER

S.No	Experiments	CO	PO
1	IDENTIFICATION OFSYSTEMLAYOUT (i) Identify front panel indicators & switches and Front side & rear side connectors (ii) Familiarize the computer system layout by marking positions of SMPS, Motherboard, FDD, HDD, CD, DVD and add on cards.	D640.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
2	HARD DISK (i) Configure bios setup program and troubleshoot the typical problems using BIOS utility.**(**ii)Install, Configure, Partition and Format Hard disk.	D640.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
3	DVD/BLU-RAYWRITER (i) Install and Configure a DVD Writer and record a blank DVD.(ii) Install and Configure a Blu-ray Writer and record a blank Blu-ray Disc	D640.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
4	Printer Installation (i)Install and configure Dot matrix printer (ii)Install and configure Laser printer	D640.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
5	(i)Install and configure Scanner (ii)Install and configure Web cam and bio-metric device	D640.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
6	(i)Assemble a system with add on cards and check the working condition of the system.(ii)Install OS in the assembled system	D640.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
7	Install Dual OS in a system	D640.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
8	(i)Assemble and Disassemble a Laptop to identify the parts.(ii)Installation of different device drivers and Installation of different Application Software.	D640.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
9	Do the following Cabling works for establishing a network (i)Crimp the network cable with RJ 45 connector in Standard cabling mode and cross cabling mode.(ii)Test the crimped cable using a cable tester	D640.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
10	Use IPCONFIG, PING, TRACERT and NETSTAT utilities to debug the network issues	D640.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
11	Interface two PCs to form Peer To Peer network using the connectivity devices Switch or Router in a LAN	D640.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
12	(i)Share the files and folders in a LAN(ii)Share a printer in a LAN.	D640.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7

13	Remote Desktop, Remote Assistance, Telnet, HyperTerminal, Team Viewer	D640.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
14	Configure DNS to establish interconnection between systems and describe how a name is mapped to IP Address	D640.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
15	(i)Install and configure Network Devices: HUB, Switch (4/8/16/24ports),Routers ii) Install and Configure NIC	D640.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
16	Install and configure DHCP server	D640.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
17.	**Mini Project**	D640.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7

ECD651 TELEVISION ENGINEERING PRACTICAL

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester: 16 Weeks

Course	Instruction		Examination			
Television Engineering Practical	Hrs. Week	Hrs Semester	Marks			
	5	80	Internal Assessment	Autonomous Examination	Total	Duration
			25	100*	100	3Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

DETAILED ALLOCATION OF MARKS

S.No	DESCRIPTION	MARKS
1	CIRCUIT DIAGRAM	25
2	CONNECTION	25
3	EXECUTION & HANDLING OF EQUIPMENT	25
4	OUTPUT /RESULT	10
5	VIVA–VOCE	5
6	MINI PROJECT	10
	TOTAL	**100**

Mini Project Evaluation (10 marks)

Breakup Details

1	Project Description	05
2	Project Demo	05
	Total	**10**

COURSE DESCRIPTION:

The introduction of this course will enable the students to get familiar with basic methods used for trouble shooting, servicing and measurement. The Simple methods are used to find the faults in the servicing of TV. The students can find the career in servicing.

EQUIPMENTS REQUIRED: (FOR A BATCH OF 30 STUDENTS)

S. No	Name of the Equipments	Required Nos
1.	Antenna elements (dipole , reflector, director)	2 Sets
2.	Audio oscillator	5 Nos
3.	CRO	2 Nos
4.	Power Supply (0 – 30v)	5 Nos
5.	Multi meters	5 Nos
6.	SMPS	4 Nos
7.	IR TV remote receivers	2 Nos
8.	B/W Television Receiver Trainer kit	-
9.	Color TV Receiver Trainer kit	-
10.	VGA Monitors	2 Nos
11.	LCD / LED monitors	2 Nos

OBJECTIVES:

The students are able to

- Understand the assembling of Antenna.
- Construct and test the deflection circuits.
- Construct and test the sync circuits.
- Service TV remote.
- Check faults in power supply.
- Find the faults in video section and audio section.
- Understand about DTH connection.
- Study the use of set of box.
- Service the monitors.
- Develop the mini project.

COURSE OUTCOMES

Course	**ECD651 TELEVISION ENGINEERING PRACTICAL**
After successful completion of this course, the students should be able to	
D651.1	Know the assembling of Yagi Uda antenna, Construct and test the sync separator circuit ,horizontal and vertical sawtooth generator.
D651.2	Troubleshooting and fault finding IR TV remote control unit, SMPS Troubleshooting of EHT and sound section in TV.
D651.3	Know the RF Tuner, trouble shooting of deflection yoke with controls.
D651.4	Know the servicing of computer monitors, LED/LCD and measure the DC voltages at various points in TV receiver.
D651.5	Identify the different components and sections in TV Receiver and develop mini project with report.

ECD651 TELEVISION ENGINEERING PRACTICAL

Note: At least 9experiments should be constructed using breadboard

1. Assembling of yagi uda antenna.
2. Construct and test the sync separator circuit.
3. Construct a horizontal saw tooth generator and measure its frequency.
4. Construct a vertical saw tooth generator and measure its frequency.
5. Trouble shooting of IR TV Remote control unit.
6. Fault finding in SMPS and measure its different voltage levels.
7. Trouble shooting of EHT section in TV.
8. Trouble shooting of sound section in TV.
9. Study of RF Tuner.
10. Trouble shooting of deflection yoke with controls.
11. Servicing of computer monitors (observe the VGA signals using CRO) .
12. Servicing of LED /LCD monitors.
13. Measure the dc voltages at various points in TV receiver.
14. Identify the different components and sections in TV Receiver.
15. Mini Project

The mini project is activity based and it may be given to group of maximum of six students for hands on experience and to create scientific temper

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:

a) Attendance (Award of marks same as theory courses)	:	05 Marks
b) Procedure/ observation and tabulation/ Other Practical related Work	:	05 Marks
c)Tests	:	10 Marks
d) Student Centered Learning (SCL) work sheet	:	05 Marks

Total		25 Marks

LEARNING WEBSITES

1. https://sites.google.com/a/hg.books-now.com/en65/9781136125171-79lustpeGEhaere93
2. https://www.britannica.com/technology/television-technology
3. http://ggpbilaspur.ac.in/Download%20Content/Download%20LAB%20MANUALS%20VIVA/Electronics%20&%20Telecommunication%20Deptt/Communication%20lab/Television%20Engg.%20%20Lab%20Manual.pdf
4. https://www.scientechworld.com/education-software-training-and-skill-development/engineering-and-vocational-products/understanding-led-television
5. https://www.ti.com/solution/smps-power-supply-for-tv

CO- POs & PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
D651.1	3	3	3	3	3	3	3	3	3	3
D651.2	3	3	3	3	3	3	3	3	3	3
D651.3	3	3	3	3	3	3	3	3	3	3
D651.4	3	3	3	3	3	3	3	3	3	3
D651.5	3	3	3	3	3	3	3	3	3	3
D651Total	15	15	15	15	15	15	15	15	15	15
Correlation Level	3	3	3	3	3	3	3	3	3	3

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

ECD651 TELEVISION ENGINEERING PRACTICAL

MODEL QUESTION PAPER

S.No	Experiments	CO	PO
1	Construct a vertical saw tooth generator for the frequency of 50 hz and verify its output	D651.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
2	Troubleshoot the sound section in TV receiver and observe the values	D651.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
3	Troubleshoot the deflection yoke of TV receiver and draw the observed waveforms	D651.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
4	Troubleshoot the EHT section of TV receiver and measure the values	D651.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
5	Construct and test the sync separator circuit and observe the waveforms and draw	D651.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
6	Assemble the Yagi-uda antenna with the given antenna elements	D651.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
7	Service the given computer monitor and observe the VGA signals using CRO	D651.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
8	Service the TV remote and find the fault	D651.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
9	Troubleshoot the given LED / LCD monitor and find the faults	D651.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
10	Service the given SMPS and measure the voltage levels	D651.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
11	Construct the horizontal saw tooth generator for the frequency of 15,625 Hz and verify its output.	D651.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
12	Measure and write down the Voltage levels of the TV receiver given for troubleshooting	D651.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
13	Study the given RF tuner and explain the function of sections of RF tuner	D651.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
14	Identify the different components and sections in TV Receiver	D651.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
15	**Mini Project**	D651.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7

ECD652 MOBILE AND OPTICAL COMMUNICATION PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

No. of weeks per semester: 16 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/Week	Hrs / Semester	Internal Assessment	Autonomous Examination	Total	
Mobile and Optical Communication	**5**	80	25	100*	100	3 Hrs

***Examinations will be conducted for 100 marks and it will be reduced to 75 marks.**

DETAILED ALLOCATION OF MARKS

S. No	DESCRIPTION	MARKS
1	CIRCUITDIAGRAM	25
2	CONNECTION	25
3	EXECUTION & HANDLING OF EQUIPMENT	25
4	OUTPUT /RESULT	10
5	VIVA–VOCE	5
6	MINI PROJECT	10
	TOTAL	100

Mini Project Evaluation (10 marks)

Breakup Details

1	Project Description	05
2	Project Demo	05
	Total	**1**

COURSE DESCRIPTION:

All types of Mobile Communication circuits are merged with Optical fiber links to get Broad band services to Home and all working environments. Hence in this Course Mobile Communication and Optical Communication related practical circuits are going to be tested by the students. By Practicing the following experiments the students can develop their skill which could be helpful for their self employment in future.

LIST OF EQUIPMENTS: (FOR A BATCH OF 30 STUDENTS)

S.NO	Name of the Equipment	Range	Required No.
1	Regulated Power Supply	0 – 30V	2
2	Dual trace CRO	60 MHz	5
3	Signal Generator	-	5
4	Desk Top Computer	-	2
5	Smart phone Tech book	-	3
6	Digital Trainer Kit	-.	2
7	Digital Multimeter	-	5

OBJECTIVES:

On completion of the following experiments, the students must be able to

- Understand the concept of Mobile Communication.
- Know the working principle of Mobile Networks.
- Know the working of Transmitter and Receiver in GSM.
- Study the working of SIM card in GSM handset andSIM card detection.
- Study and observe Transmitted/Received RF signal.
- Study and observe Transmitted(I&Q)/Received (I&Q)signals constellations.
- Study and analyze the Buzzer in 4GLTE Smart Phone Tech Book.
- Study and Analyze the Vibrator in 4GLTE Smart Phone Tech Book.
- Study of switch faults in User Interface Section of 4GLTE Smart Phone Tech Book.
- Study and analyze the Power Management Unit in 4GLTE Smart Phone Tech Book.
- Generate the Pseudo random binary sequence.
- Test the VI characteristics of LED (Light emitter) and Photo diode (Light detector).
- Test the VI Characteristics of an Opto – coupler.
- Test the performance of Time Division Multiple Access in Fiber optical communication link.
- Determine the Numerical aperture of the given optical fiber.
- Develop the mini project.

COURSE OUTCOMES

Course	**ECD652 MOBILE AND OPTICAL COMMUNICATION**
After successful completion of this course, the students should be able to	
D 652.1	Know the working of SIM card in GSM handset and SIM card detection , observing transmitted and received RF signals , I & Q signal constellations.
D 652.2	Understand buzzer and vibrator in 4GLTE Smartphone tech book.
D 652.3	Know the switch fault in user interface section and power management unit of 4GLTE Smart phone tech book and pseudo random binary sequence.
D 652.4	Construct and test VI characteristics of LED, Photo diode and opto coupler.
D 652.5	Test the performance of TDM in OFC, Numerical aperture of optical fibre coupling loss in optical fiber and develop mini project with report.

ECD652 MOBILE AND OPTICAL COMMUNICATION PRACTICAL

MOBILE COMMUNICATION

(To understand the Basic circuit of Mobile phone (Transmitter, Receiver and Baseband control Section).

1. To study the working of SIM card in GSM hand set and SIM card detection.
2. To Study and observe Transmitted/Received RF signal.
3. Study and observe Transmitted (I&Q)/Received (I&Q) signals constellations.
4. Study and analyze the Buzzer in 4GLTE Smart Phone Tech Book.
5. To study and Analyze the Vibrator in 4GLTE Smartphone Tech Book
6. Study of switch faults in User Interface Section of 4GLTE Smart Phone Tech Book
7. Study and analyze the Power Management Unit in 4GLTE Smart Phone Tech Book
8. Generation of Pseudo random binary sequence

OPTICAL COMMUNICATION

9. Construct a circuit to test the VI characteristics of LED (Light emitter) and Photodiode(Light detector)
10. Construct a circuit to test the VI Characteristics of an Opto -coupler
11. Test the performance of Time Division Multiple Access in Fiber optical communication link
12. Determine the Numerical aperture of the given optical fiber
13. Determine the Coupling loss in optical fiber with two different fiber length.
14. Mini Project

The mini project is activity based and it may be given to group of maximum of six students for hands on experience and to create scientific temper.

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:

a) Attendance (Award of marks same as theory courses)	:	05 Marks
b) Procedure/ observation and tabulation/ Other Practical related Work	:	05 Marks
c)Tests	:	10 Marks
d) Student Centered Learning (SCL) work sheet	:	05 Marks
Total		25 Marks

LEARNING WEBSITE

1. http://vlabs.iitkgp.ernet.in/fcmc/
2. http://vlabs.iitkgp.ac.in/fcmc/exp8/index.html#
3. https://www.dbit.ac.in/ece/syllabus/optical-fiber-communication-lab.pdf
4. https://www.thefoa.org/PPT/LabManual.pdf
5. https://www.allaboutcircuits.com/projects/category/telecom/optical-communication

CO- POs & PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
D652.1	3	3	3	3	3	3	3	3	3	3
D652.2	3	3	3	3	3	3	3	3	3	3
D652.3	3	3	3	3	3	3	3	3	3	3
D652.4	3	3	3	3	3	3	3	3	3	3
D652.5	3	3	3	3	3	3	3	3	3	3
D652Total	15	15	15	15	15	15	15	15	15	15
Correlation Level	3	3	3	3	3	3	3	3	3	3

Correlation level 1- Slight (low)

Correlation level 2- Moderate (Medium)

Correlation level 3- Substantial (high)

ECD652 MOBILE AND OPTICAL COMMUNICATION

MODEL QUESTION PAPER

S.No	Experiments	CO	PO
1	Study the working of SIM card in GSM hand set and SIM card detection	D652.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
2	Study and observe Transmitted/Received RF signal	D652.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
3	Study and observe Transmitted (I&Q) /Received (I&Q) signals constellations	D652.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
4	Study and analyze the Buzzer in 4GLTE Smart Phone Tech Book	D652.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
5	Study and Analyze the Vibrator in 4GLTE Smart phone Tech Book	D652.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
6	Study of switch faults in User Interface Section of 4GLTE Smart Phone Tech Book	D652.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
7	Study and analyze the Power Management Unit in 4GLTE Smart Phone Tech Book	D652.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
8	Generate Pseudo random binary sequence	D652.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
9	Construct a circuit to test the VI characteristics of LED (Light emitter) and Photo diode (Light detector)	D652.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
10	Construct a circuit to test the VI Characteristics of an Opto – coupler	D652.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
11	Test the performance of Time Division Multiple Access in Fiber optical communication link	D652.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
12	Determine the Numerical aperture of the given optical fiber	D652.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
13	Determine the Coupling loss in optical fiber with two different fiber length.	D652.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
14	**Mini Project**	**D652.5**	**PO1,PO2,PO3,PO4, PO5,PO6,PO7**

ECD653 EMBEDDED SYSTEMS PRACTICAL

TEACHINGAND SCHEME OFEXAMINATION

No.of weeks/ Semester: 16weeks

Course	Instruction		Examination			
			Marks			Duration
	Hours /week	Hours /semester	Internal Assessment	Autonomous Examination	Total	
Embedded Systems practical	5	80	25	100*	100	3 Hours

*** Examination will be conducted for 100 marks and it will be reduced to 75 marks.**

DETAILED ALLOCATION OF MARKS

S.NO	DESCRIPTION	MARKS
1	ALGORITHM/FLOW CHART	20
2	PROGRAM	25
3	EXECUTION OF PROGRAM	30
4	OUTPUT /RESULT	10
5	VIVA–VOCE	5
6	MINI PROJECT	10
	TOTAL	**100**

Mini Project Evaluation (10 marks)

Breakup Details

1	Project Description	05
2	Project Demo	05
	Total	**10**

COURSE DESCRIPTION:

The introduction of this course will enable the students to have hands on experience in using ARM Based trainer kit. The students are exposed to use the on chip peripherals using embedded C language. They can also get familiar with the use of ARM instruction set. They are learning the different methods for providing time delay and use of serial communication. 32 bit ARM is a RISC processor which makes the students to expose to the new dimension in the field of embedded systems

LIST OF EQUIPMENTS: (FOR A BATCH OF 30 STUDENTS)

S.No	Name of the Equipments	Required Nos.
1	ARM 7 TDMI KIT(TMS 4701,LPC2138,LPC2148 or STR7)	15 Nos
2	Desktop computer/Laptop	15 Nos
3	Interfaces: Seven Segment display LEDS switches and stepper motor	Each 01

OBJECTIVES:

The students are able to

- Understand the use of instruction set by writing simple ARM ALP and simulate to see output.
- Know the application details of on chip peripherals.
- Familiarize with the register map of on chip Timer / counter.
- Know the use of serial communication concepts using on chip UART0.
- Understand the use of GPIO and the connection of peripheral devices using these on chip GPIO programmable port Pins.
- Use the interrupts with the help of VIC.
- Get used with pin connect block registers for programming the GPIO port pins.
- Interface stepper motor and its operation.
- Understand the multiplexing of seven segment LED display device.
- Develop the mini project.

COURSE OUTCOMES

Course	**ECD 653 EMBEDDED SYSTEMS PRACTICAL**
After successful completion of this course, the students should be able to	
D 653.1	Familiarize about ARM processor kit and simulate arithmetic operation, soft delay and LED blinking with variable speed.
D 653.2	Realize the input and output port in ARM ,timer peripheral in ARM by polling method and timer peripheral in ARM by interrupt driven method. To read the switch and display in the LEDs. To display a number in seven segment LED.
D 653.3	Write C Program and execute serial transmission and reception of a character by interrupt method(UART), To count external interrupt pulses EINTx .
D 653.4	Write a C program for accessing an internal ADC and To generate square wave using on chip DAC.
D 653.5	ARM Processor to run a timer Peripheral Using Polling Method and develop mini project with report.

ECD653 EMBEDDED SYSTEMS PRACTICAL

1. Study of ARM Processor kit.(Example LPC 2148 kit)
2. Write assembly language program for addition, subtraction and multiplication and simulate.
3. Write and execute C program to blink the LEDs using software delay routine.
4. Write and execute C program to blink the LEDs using on chip TIMER// COUNTER for the delay(Using Polling method).
5. Write and execute C program to blink the LEDs using on chip TIMER// COUNTER for the delay(Using interrupt method).
6. Write and execute C program to read the switch and display in the LEDs.
7. Write and execute C program to count external interrupt pulses EINTx (using VIC) and Show the binary count value in LEDs.
8. Write and execute C program to display a number in seven segment LED.
9. Write and execute C program for serial transmission and reception using on chip UART. Send the received character back to the PC by Polling method.
10. Write and execute C program for serial transmission and reception using on chip UART. Send the received character back to the PC by Interrupt method.
11. Write and execute C program for accessing an internal ADC and display the binary output in LEDs.
12. Write and execute C program to generate square wave using on chip DAC.
13. Write and execute C program r to run a timer peripheral using polling method.
14. Mini Project

The mini project is activity based and it may be given to group of maximum of six students for hands on experience and to create scientific temper.

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:

a) Attendance (Award of marks same as theory courses)	:	05 Marks
b) Procedure/ observation and tabulation/ Other Practical related Work	:	05 Marks
c)Tests	:	10 Marks
d) Student Centered Learning (SCL) work sheet	:	05 Marks

Total		25 Marks

LEARNING WEBSITES

1. https://muresults.net/itacademic/Workshopdata/ES.pdf
2. http://www.inf.ed.ac.uk/teaching/courses/es/PDFs/Coursework-2.pdf
3. http://vlabs.iitkgp.ernet.in/rtes/
4. https://sites.google.com/site/coolembeddedlaboratory/

CO- POs & PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
D 653.1	3	3	3	3	3	3	3	3	3	3
D 653.2	3	3	3	3	3	3	3	3	3	3
D 653.3	3	3	3	3	3	3	3	3	3	3
D 653.4	3	3	3	3	3	3	3	3	3	3
D 653.5	3	3	3	3	3	3	3	3	3	3
D 653Total	15	15	15	15	15	15	15	15	15	15
Correlation Level	3	3	3	3	3	3	3	3	3	3

ECD653 EMBEDDED SYSTEMS PRATICAL

MODEL QUESTION PAPER

S.No	Experiments	CO	PO
1	Write a C program to blink a LED with the time delay of 1 second. Time delay can be generated using software delay routine.	D653.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
2	Write a C program to blink the LEDs with the time delay. Generate the time delay using internal TIMER in polling method and verify.	D653.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
3	Write a C program to display the following single digit number----------at seven segment LED device.	D653.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
4	Write a C program using on chip UART for serial transmission and reception using polling method and check the output.	D653.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
5	Write an assembly language program to add /subtract 32 bit numbers and simulate the output result.	D653.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
6	Write a C program to blink the LEDs with the time delay. Generate the time delay using internal TIMER in interrupt method and verify.	D653.2	PO1,PO2,PO3,PO4, PO5,PO6,PO7
7	Write a C program using on chip UART for serial transmission and reception using interrupt method and check the output.	D653.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
8	Write a C program to convert analog signal to digital using internal ADC and verify the binary output at the LEDs.	D653.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
9	Write a C program to use the internal DAC to generate a square wave output and observe the output at CRO.	D653.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
10	Write a C program to get the input from the a switch and display at the LEDs.	D653.4	PO1,PO2,PO3,PO4, PO5,PO6,PO7
11	Write a C program to demonstrate the use of external interrupt using on chip VIC and observe the at the LEDs.	D653.3	PO1,PO2,PO3,PO4, PO5,PO6,PO7
12	Write an assembly language program to multiply two numbers and simulate the output result.	D653.1	PO1,PO2,PO3,PO4, PO5,PO6,PO7
13	Write and execute C program r to run a timer peripheral using polling method.	D653.5	PO1,PO2,PO3,PO4, PO5,PO6,PO7
14	**Mini Project**	**D653.5**	**PO1,PO2,PO3,PO4, PO5,PO6,PO7**

ECD660 PROJECT WORK & INTERNSHIP

TEACHING AND SCHEME OF EXAMINATION

No. of weeks per semester: 16 weeks

Course	Instruction		Examination			
	Hrs/Week	Hrs / Semester	Marks			Duration
			Internal Assessment	Autonomous Examination*	Total	
PROJECT WORK & INTERNSHIP	6	96	25	100*	100	3 Hrs

*Examination will be conducted for 100 marks and it will be reduced to 75 marks.

Minimum Marks for Pass is 50 out of which minimum 50 marks should be obtained out of 100 marks in the Autonomous Examination alone.

OBJECTIVES:

- The project work and internship is aimed to assemble test a photo type model of any one item/gadget.
- Real time application problems if any may be identified from any industry and may be chosen.
- The knowledge and the skill so far acquired may be made use of.
- The team spirit may be motivated.
- The entrepreneurship ideas may be motivated by conducting a career guidance programme.
- Learn and understand the gap between the technical knowledge acquired through curriculum and the actual industrial need through internship and to compensate it by acquiring additional knowledge as required.

COURSE OUTCOMES

Course	ECD 660 PROJECT WORK & INTERNSHIP
After successful completion of this course, the students should be able to	
D660.1	Identify Real time application problems and apply the acquired knowledge and skills to solve it.
D660.2	Assemble and test a proto type model.
D660.3	Understand the team spirit and get motivated.
D660.4	Get the entrepreneurship ideas through career guidance programme.
D660.5	Learn and understand the gap between the technological knowledge acquired through curriculum and the actual industrial needs through internship and to compensate it by acquiring additional knowledge as required.

CONTINUOUS INTERNAL ASSESSMENT:

The internal assessment should be calculated based on the review of the progress of the work done by the student periodically as follows.

Detail of assessment	Period of assessment	Max. Marks
First Review	6th week	10
Second Review	12th week	10
Attendance	Entire semester	5
Total		**25**

EVALUATION FOR AUTONOMOUS EXAMINATION:

Details of Mark allocation	Max Marks
Demonstration/Presentation	25
Report	25
Viva Voce	30
Internship report	20
Total	100

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
D660.1	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
D660.2	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
D660.3	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
D660.4	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
D660.5	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
D660	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**
Correlation Level	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**

Correlation level 1 – Slight (low)
Correlation level 2 – Moderate (Medium)
Correlation level 3–Substantial (high)

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ECD610 COMPUTER HARDWARE SERVICING AND NETWORKING

MODEL QUESTION PAPER

Time: 3 Hrs **Max.Marks:100**

PART-A (10 X 3 = 30Marks)					
Note: Answer all questions. All questions carry equal marks					
S.No	**Questions**	**UNIT**	**Bloom's Level**	**CO**	**PO**
1	What are Hardware and software?	I	R	D610.1	PO1,PO2
2	What is primary Memory?	I	R	D610.1	PO1,PO2
3	State the different types of I/O ports.	II	U	D610.2	PO1,PO2
4	What is UPS ?and mention its types.	II	R	D610.2	PO1,PO2
5	What is BIOS?	III	R	D610.3	PO1,PO2
6	What is Anti-Virus?	III	R	D610.3	PO1,PO2
7	List out the differences between simplex and Half duplex.	IV	U	D610.4	PO1,PO2
8	Define Topologies.	IV	R	D610.4	PO1,PO2
9	Write short note on IGMP.	V	U	D610.5	PO1,PO2
10	Write about cloud computing.	V	U	D610.5	PO1,PO2

	PART-B (5 X 14 = 70 Marks)					
	Note: Answer all questions choosing A or B in each question. All questions carry equal marks					
S.No	**Questions**	**Marks**	**UNIT**	**Bloom's Level**	**CO**	**PO**
11	(A) (i) Explain the construction, reading and writing operations of DVD-RW.	07	I	U	D610.1	PO1,PO2,PO3
	(ii) Explain construction and working principle of hard disk.	07	I	U	D610.1	PO1,PO2,PO3
	(OR)					
	(B) (i) Explain architecture and block diagram of multicore processor.	07	I	U	D610.1	PO1,PO2,PO3
	(ii) Explain primary memory and cache memory.	07	1	U	D610.1	PO1,PO2,PO3

12	(A) (i) With a neat block diagram, explain working of ON LINE UPS.	07	II	U	D610.2	PO1,PO2,PO3
	(ii) With a neat block diagram, explain working of OFF LINE UPS	07	II	U	D610.2	PO1,PO2,PO3
	(OR)					
	(B) (i) Explain the working of mechanical keyboard with suitable diagram.	07	II	U	D610.2	PO1,PO2,PO3
	(ii) Explain the operation of optical mouse.	07	II	U	D610.2	PO1,PO2,PO3
13	(A).(i) With a neat block diagram, explain laptop mother board	07	III	U	D610.3	PO1,PO2,PO3
	(ii) Explain (a) Beep codes (b) Firewalls	07	III	U	D610.3	PO1,PO2,PO3
	(OR)					
	(B) (i)Explain BIOS in detail.	07	III	U	D610.3	PO1,PO2,PO3
	(ii) Explain Computer virus, precautions and identifying its signature.	07	III	U	D610.3	PO1,PO2,PO3
14	(A) (i) Explain about topologies used in computer network.	07	IV	U	D610.4	PO1,PO2,PO3
	(ii) Explain (a) Client – server network (b) Gateways	07	IV	U	D610.4	PO1,PO2,PO3
	(OR)					
	(B) (i) Explain in detail about networks and its types	07	IV	U	D610.4	PO1,PO2,PO3
	(ii) Explain (i) Half duplex (ii) Full Duplex	07	IV	U	D610.4	PO1,PO2,PO3
15	(A) (i) Explain about (a) HTTP (b) DNS (c) POP	07	V	U	D610.5	PO1,PO2,PO3
	(ii) Explain about (a)FTP (b) Telnet.	07	V	U	D610.5	PO1,PO2,PO3
	(OR)					
	(B) (i) Explain 802.X Protocol in detail	07	V	U	D610.5	PO1,PO2,PO3
	(ii) Explain (a) Token ring protocol(b)IGMP	07	V	U	D610.5	PO1,PO2,PO3

QUESTION PAPER SETTING

The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as Presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD620 BIOMEDICAL INSTRUMENTATION

MODEL QUESTION PAPER

TIME: 3hours **MARKS: 100**

PART-A (10 X 3 = 30Marks)					
Note: Answer all questions. All questions carry equal marks					
S.No	**Questions**	**UNIT**	**Bloom's Level**	**CO**	**PO**
1	What are electrodes? List the various types of electrodes.	I	R	D620.1	PO1 ,PO2
2	What are the value of Systolic and Diastolic blood pressure?	I	R	D620.1	PO1 ,PO2
3	Draw the various types of EEG wave. Mention the frequency range of each type.	II	U	D620.2	PO1 ,PO2
4	What do you mean by Air conduction and Bone conduction test?	II	R	D620.2	PO1 ,PO2
5	What are the various processes involved in Dialysis?	III	R	D620.3	PO1 ,PO2
6	What is the necessity of Ventilators?	III	R	D620.3	PO1 ,PO2
7	Define: (i) Macro shock (ii) Micro shock	IV	U	D620.4	PO1 ,PO2
8	What are the concepts of Telemedicine?	IV	R	D620.4	PO1 ,PO2
9	List any two applications of LASER in medical field.	V	U	D620.5	PO1 ,PO2
10	Differentiate CT scan with MRI scan.	V	U	D620.5	PO1 ,PO2

	PART-B (5 X 14 = 70 Marks)					
	Note: Answer all questions choosing A Or B in each question. All questions carry equal marks					
S.No	**Questions**	**Marks**	**UNIT**	**Bloom's Level**	**CO**	**PO**
11	A. (i). Explain the working of Ultrasonic blood flow meter.	07	I	U	D620.1	PO1, PO2,PO3
	(ii). Explain (i) Resting Potential (ii)Action Potential.	07	I	U	D620.1	PO1, PO2,PO3
	(OR)					
	B. (i). Explain the working of Spirometer	07	I	U	D620.1	PO1, PO2,PO3

	(ii). Explain the Sphygmomanometer method of BP measurement.	07	1	U	D620.1	PO1, PO2,PO3
12	A. (i). Explain the working of ECG machine.	07	II	U	D620.2	PO1, PO2,PO3
	(ii). Explain 10-20 EEG lead system.	07	II	U	D620.2	PO1, PO2,PO3
	(OR)					
	B. (i). Explain how Conduction Velocity can measured using EMG Machine.	07	II	U	D620.2	PO1, PO2,PO3
	(ii) Explain the working of Basic Audiometer.	07	II	U	D620.2	PO1, PO2,PO3
13	A. (i). Explain the working of Programmable Pacemaker.	07	III	U	D620.3	PO1, PO2,PO3
	(ii). Explain the working of Heart Lung machine.	07	III	U	D620.3	PO1, PO2,PO3
	(OR)					
	B.(i). Explain the working of Hemo dialyser.	07	III	U	D620.3	PO1, PO2,PO3
	(ii). Explain the working of Lithotripter.	07	III	U	D620.3	PO1, PO2,PO3
14	A.(i) Explain the Hazardous situations of Macro shock and Micro shock	07	IV	U	D620.4	PO1, PO2,PO3
	(ii) Explain the working Single channel radio telemetry system.	07	IV	U	D620.4	PO1, PO2,PO3
	(OR)					
	B.(i). Explain the working Ground Fault Interrupter	07	IV	U	D620.4	PO1, PO2,PO3
	(ii). What are the Physiological Effects of electric current.	07	IV	U	D620.4	PO1, PO2,PO3
15	A.(i). Explain the working of X –Ray apparatus	07	V	U	D620.5	PO1, PO2,PO3
	(ii). Explain the working of Magnetic Resonance Imaging.	07	V	U	D620.5	PO1, PO2,PO3
	(OR)					
	B.(i)Explain about Pulse echo system	07	V	U	D620.5	PO1,

						PO2,PO3
	(ii) Explain about Positron Emission Tomography.	07	V	U	D620.5	PO1, PO2,PO3

QUESTION PAPER SETTING

The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as Presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD631 TELEVISION ENGINEERING

MODEL QUESTION PAPER

TIME: 3hours **MARKS: 100**

PART-A (10 X 3 = 30Marks)					
Note: Answer all questions. All questions carry equal marks					
S.No	**Questions**	**UNIT**	**Bloom's Level**	**CO**	**PO**
1	What is meant by flicker? How can it be eliminated?	I	R	D631.1	PO1, PO2
2	Draw the composite video signal.	I	U	D631.1	PO1, PO2
3	Define hue, saturation, Luminance and Chrominance.	II	U	D631.2	PO1, PO2
4	What is meant by automatic degaussing?	II	R	D631.2	PO1, PO2
5	Compare Low level and high level modulation.	III	U	D631.3	PO1, PO2
6	List out the requirements of Video amplifier.	III	R	D631.3	PO1, PO2
7	Write the merits of LED TV.	IV	R	D631.4	PO1, PO2
8	What is the use of set top box?	IV	R	D631.4	PO1, PO2
9	Write down the applications of CCTV.	V	R	D631.5	PO1, PO2
10	Write about HDTV.	V	R	D631.5	PO1, PO2

	PART-C (5 X 14 = 70 Marks)					
	Note: Answer all questions choosing A or B in each question. All questions carry equal marks					
S.No	**Questions**	**Marks**	**UNIT**	**Bloom's Level**	**CO**	**PO**
11	A.(i). Draw the basic block diagram of TV transmitter and receiver and explain	07	I	U	D631.1	PO1,

	briefly.					PO2,PO3
	(ii). Explain Interlaced scanning.	07	I	U	D631.1	PO1, PO2,PO3
	(OR)					
	B. (i). Explain the formation of chrominance signal in PAL system.	07	I	U	D631.1	PO1, PO2,PO3
	(ii). Draw the composite video signal and explain.	07	1	U	D631.1	PO1, PO2,PO3
12	A. (i). Draw and explain the Principle of operation of Vidicon Camera tube.	07	II	U	D631.2	PO1, PO2,PO3
	(ii). Explain the operation of CCD Camera.	07	II	U	D631.2	PO1, PO2,PO3
	(OR)					
	B. (i). Draw and explain the working principle of Trinitron color picture tube.	07	II	U	D631.2	PO1, PO2,PO3
	(ii) Draw the block diagram of color TV camera tube and explain.	07	II	U	D631.2	PO1, PO2,PO3
13	A. (i). Draw and explain the block diagram of Low level IF modulated visual exciter.	07	III	U	D631.3	PO1, PO2,PO3
	(ii). Draw and explain the operation of CIN diplexer.	07	III	U	D631.3	PO1, PO2,PO3
	(OR)					
	B.(i). Draw the PAL color receiver block diagram.	07	III	U	D631.3	PO1, PO2,PO3
	(ii). Explain low and high frequency compensation.	07	III	U	D631.3	PO1, PO2,PO3
14	A.(i) Explain the working principle of LCD TV with neat diagram.	07	IV	U	D631.4	PO1, PO2,PO3
	(ii) Explain the principle of operation of Plasma TV.	07	IV	U	D631.4	PO1, PO2,PO3
	(OR)					
	B.(i). Explain the working principle of LED TV with diagram	07	IV	U	D631.4	PO1, PO2,PO3
	(ii).Explain the principle of operation of Flat panel Display.	07	IV	U	D631.4	PO1, PO2,PO3

15	A.(i).Draw the block diagram of Digital color TV receiver.	07	V	U	D631.5	PO1, PO2,PO3
	(ii).Explain the operation of digital CCD tele cine system with diagram.	07	V	U	D631.5	PO1, PO2,PO3
	(OR)					
	B. (i). Draw and explain remote control IR Transmitter and Receiver.	07	V	U	D631.5	PO1, PO2,PO3
	(ii). Explain CCTV in detail.	07	V	U	D631.5	PO1, PO2,PO3

QUESTION PAPER SETTING

The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as Presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD632 MOBILE AND OPTICALCOMMUNICATION

MODEL QUESTION PAPER

TIME: 3hours **MARKS: 100**

PART-A (10 X 3 = 30Marks)					
Note: Answer all questions. All questions carry equal marks					
S.No	**Questions**	**UNIT**	**Bloom's Level**	**CO**	**PO**
1	State the methods of improving coverage.	I	R	D632.1	PO1,PO2
2	What do you mean by Hand off?	I	R	D632.1	PO1,PO2
3	What are the various methods of Diversity?	II	R	D632.2	PO1,PO2
4	What is the importance of Channel coding?	II	R	D632.2	PO1,PO2
5	What is the difference between Wireless networks and Fixed networks?	III	R	D632.3	PO1,PO2
6	What is UMTS?	III	R	D632.3	PO1,PO2
7	Define Coupling Efficiency.	IV	R	D632.4	PO1,PO2
8	What are the various methods of Splicing?	IV	R	D632.4	PO1,PO2
9	What do you mean by Optical CDMA?	V	R	D632.5	PO1,PO2
10	List any two advantages of Wavelength Routed Networks.	V	R	D632.5	PO1,PO2

	PART-B (5 X 14 = 70 Marks)					
	Note: Answer all questions choosing A or B in each question. All questions carry equal marks					
S.No	**Questions**	**Marks**	**UNIT**	**Bloom's Level**	**CO**	**PO**
11	A.(i). Explain about Hand off Strategies.	07	I	U	D632.1	PO1,PO2,PO3
	(ii). Explain how Co-channel interference affects System capacity.	07	I	U	D632.1	PO1,PO2,PO3
	(OR)					
	B. (i). Explain about Channel Assessment Strategies.	07	I	U	D632.1	PO1,PO2,PO3
	(ii). Explain the concept of Micro cell.	07	1	U	D632.1	PO1,PO2,PO3
12	A. (i). Explain the working of an Adaptive Equalizer at the receiver of a simplified Communication System.	07	II	U	D632.2	PO1,PO2,PO3
	(ii). Differentiate between LTE and VoLTE.	07	II	U	D632.2	PO1,PO2,PO3
	(OR)					
	B. (i). Explain the working of GSM Speech encoder .	07	II	U	D632.2	PO1,PO2,PO3
	(ii) Explain the working of RAKE Receiver.	07	II	U	D632.2	PO1,PO2,PO3
13	A. (i). Explain the working of CDPD Network.	07	III	U	D632.3	PO1,PO2,PO3
	(ii). Explain the working of Common Channel Switching Network Architecture.	07	III	U	D632.3	PO1,PO2,PO3
	(OR)					

	B.(i). Explain the working of Cellular Packet Switched Architecture.	07	III	U	D632.3	PO1,PO2,PO3
	(ii). Explain the working of first generation wireless network.	07	III	U	D632.3	PO1,PO2,PO3
14	A.(i) Explain the Simplex point to point transmission link.	07	IV	U	D632.4	PO1,PO2,PO3
	(ii) Explain about Optical Fiber Cables.	07	IV	U	D632.4	PO1,PO2,PO3
	(OR)					
	B.(i). Explain about any TWO Splicing Techniques.	07	IV	U	D632.4	PO1,PO2,PO3
	(ii).Explain any two types of Connectors.	07	IV	U	D632.4	PO1,PO2,PO3
15	A.(i).Explain the working of Optical CDMA.	07	V	U	D632.5	PO1,PO2,PO3
	(ii).Explain the working of Bit – interleaved Optical TDM.	07	V	U	D632.5	PO1,PO2,PO3
	(OR)					
	B.(i) Explain the various Network Topologies.	07	V	U	D632.5	PO1,PO2,PO3
	(ii)Explain the working of SONET/ SDH Ring.	07	V	U	D632.5	PO1,PO2,PO3

QUESTION PAPER SETTING

The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as Presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECD633 EMBEDDED SYSTEMS

MODEL QUESTION PAPER

TIME: 3hours **MARKS: 100**

PART-A (10 X 3 = 30Marks)					
Note: Answer any TEN questions. All questions carry equal marks					
S.No	**Questions**	**UNIT**	**Bloom's Level**	**CO**	**PO**
1	Compare RISC and CISC.	I	U	D633.1	PO1,PO2
2	Explain Little Endian and Big Endian.	I	U	D633.1	PO1,PO2
3	Compare ARM state and Thumb state instruction.	II	U	D633.2	PO1,PO2
4	Write the classification of instruction sets.	II	R	D633.2	PO1,PO2
5	List the features of LPC 2148.	III	R	D633.3	PO1,PO2
6	Give ARM 7 nomenclature.	III	U	D633.3	PO1,PO2
7	List the features of GPIO.	IV	R	D633.4	PO1,PO2
8	Give the registers of DAC.	IV	R	D633.4	PO1,PO2
9	What is meant by Embedded OS?	V	R	D633.5	PO1,PO2
10	What is scheduler?	V	R	D633.5	PO1,PO2

	PART-B (5 X 14 = 70 Marks)					
	Note: Answer all questions choosing A or B in each question. All questions carry equal marks					
S.No	**Questions**	**Marks**	**UNIT**	**Bloom's Level**	**CO**	**PO**
11	A.(i). Draw and Explain the data flow model of ARM.	07	I	U	D633.1	PO1,PO2,PO3
	(ii). Explain the modes of operation of ARM.	07	I	U	D633.1	PO1,PO2,PO3
	(OR)					
	B. (i). Draw the block diagram of ARM based embedded system and explain.	07	I	U	D633.1	PO1,PO2,PO3
	(ii). Explain about exceptions.	07	1	U	D633.1	PO1,PO2,PO3
12	A. (i). Explain data processing instructions with examples.	07	II	U	D633.2	PO1,PO2,PO3
	(ii). Explain about software interrupt instruction set.	07	II	U	D633.2	PO1,PO2,PO3
	(OR)					

	B. (i). Explain Load store instructions with examples.	07	II	U	D633.2	PO1,PO2,PO3
	(ii) Explain about stack instructions.	07	II	U	D633.2	PO1,PO2,PO3
13	A. (i). Draw the block diagram of LPC2148 ARM controller.	07	III	U	D633.3	PO1,PO2,PO3
	(ii). Explain about VIC in detail.	07	III	U	D633.3	PO1,PO2,PO3
	(OR)					
	B.(i). Explain about memory map with detailed diagram.	07	III	U	D633.3	PO1,PO2,PO3
	(ii). What is meant by external interrupt? Explain in detail.	07	III	U	D633.3	PO1,PO2,PO3
14	A.(i) Draw the block diagram of Timer/ counter and explain its features.	07	IV	U	D633.4	PO1,PO2,PO3
	(ii) Describe the registers of GPIO.	07	IV	U	D633.4	PO1,PO2,PO3
	(OR)					
	B.(i). Draw the block diagram of PWM and explain its features.	07	IV	U	D633.4	PO1,PO2,PO3
	(ii).Explain the registers of UART0.	07	IV	U	D633.4	PO1,PO2,PO3
15	A.(i).What is scheduler? Explain pre-emptive scheduling	07	V	U	D633.5	PO1,PO2,PO3
	(ii).Explain about foreground/back ground system.	07	V	R	D633.5	PO1,PO2,PO3
	(OR)					
	B.(i) What is mutual exclusion? Explain the semaphores in detail	07	V	R	D633.5	PO1,PO2,PO3
	(ii) Explain about message queues	07	V	U	D633.5	PO1,PO2,PO3

QUESTION PAPER SETTING

The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as Presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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